FINAL REPORT

Of

THE ESTABLISHMENT OF PROCEDURES FOR THE APPLICATION OF INFRARED TECHNIQUES FOR THE ENHANCEMENT OF LARGE SCALE INTEGRATION (LSI) RELIABILITY

CONTRACT NO. NAS8-25862

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1. INTRODUCTION

The technological progress of Large Scale Integration circuits follows the sequence of steps that is common for most items in the technical field. Namely:

a) design
b) development
c) preliminary evaluation
d) development of test techniques
e) verification of adequate reliability
f) general acceptance usage

At the present time, substantial effort is applied to steps d) and e) because attainment of high reliability is one of the prerequisites for widespread LSI usage.

LSI circuits can be grouped in two basic families: MOS and Bipolars. However, from a reliability point of view, the prevalent failure causes are common to both groups. Figure 1 summarizes the observed causes of failure in MOS devices, and their percentage contribution to the total failures. This illustration was obtained from L. Hamiter's paper entitled: "Large Scale Integrated Circuits for Space Electronics".

Present test techniques encompass a wide range of operations, both in the electrical and in the mechanical fields. However,

their effectiveness is not total, so that it is impossible to prevent all early field failures. Furthermore, most of the tests are performed "after the fact"; that is, after manufacturing was completed, while it would be of interest to have the capability to monitor the quality of some key manufacturing operations at the time they are performed.

In the constant search for new and better methods to enhance reliability, the novel capabilities of recently developed infrared test equipment appeared worthy of consideration and evaluation.

The test equipment in question is the following:

the Thermal Bond Monitor

the Semiconductor Junction Analyzer

The INSPECT System

Each of these instruments can yield information of a nature that so far was either very difficult or impossible to obtain, and that can substantially help to reduce some of the causes for semiconductor failure. In particular, the Thermal Bond Monitor enables the operator to control the die-attach operation of semiconductor chips and the thermocompression wire bonding process; the Semiconductor Junction Analyzer measures, without contact, current flow through discrete semiconductor junctions; and the INSPECT System yields: 1) a computer printout representing the temperature of pre-selected points located on

a flat target placed in its focal plane; and 2) an oscilloscope display of the infrared radiation emitted by all points of the target's surface.

By implementing these capabilities, semiconductor failures can be reduced in the following areas:

semiconductor bonding to substrate;

wire bonding;

faulty electrical operation of junctions;

disclosing the presence of undesirable thermal overstresses.

It is obvious that application of these capabilities to LSI circuits will bring about substantial reliability enhancement. The purpose of the present contract was to investigate how the above-listed infrared techniques can best be applied to improve both the design and the manufacture of LSI circuits. This was successfully accomplished, as described in the present Final Report.

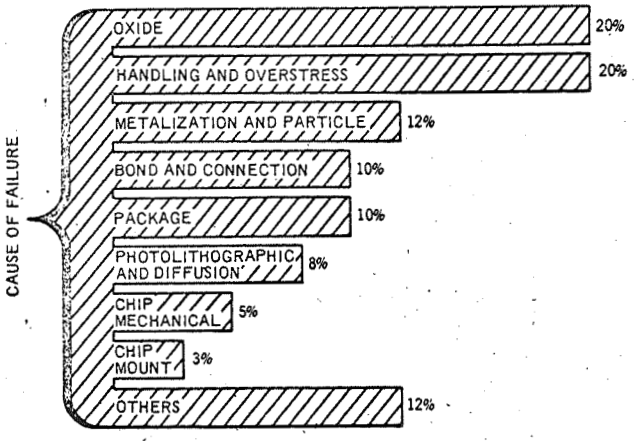

FIGURE 1. MOS Failure Causes

2. PROBLEM DEFINITION

Implementation of this program called for the following action items:

a) discussion of all major causes for LSI failure;

b) evaluation of practical applicability and usefulness of infrared techniques to each of the items discussed in a);

c) outlining feasibility programs designed to verify applicability whenever favorable results are anticipated;

d) obtaining the equipment and the semiconductors necessary to implement the programs under c);

e) carrying out the feasibility programs;

f) evaluating the results so obtained;

g) report writing.

Items a) to g) are further elaborated in the following Sections:

a) Discussion of failure causes

Figure 1 breaks down the major failure causes into nine groups, eight of which are clearly identified and connected with known failure mechanisms. These were carefully reviewed in order to determine whether infrared techniques could help in reducing the incidence of failures, either through disclosure of anomalous conditions, or through elimination of a failure cause.

In particular, as we follow the items shown in Figure 1:

2.1 Oxide Defects

These defects seem difficult to detect with infrared techniques, unless their presence would substantially affect the electrical performance of the circuits in the LSI unit. Otherwise, pinholes, variations in thickness and other mechanical defects of the silicon oxide layers would be very hard to detect.

2.2 Handling and Overstress

In this class of defects the same criteria prevails; namely only in those instances where the electrical junctions of the LSI elements are affected, infrared techniques might be able to help. However, conventional inspection and test techniques appear more appropriate for the detection of defects in this group.

2.3 Metallization and Particle

Defects in this class are more likely to be detected by infrared techniques, since their presence in most instances does affect the electrical operation of the LSI circuits and elements. In particular, the following instances should be detected, either with the use of the Semiconductor Junction Analyzer or with the use of the Fast Scan Infrared Microscope:

intra or inter level shorts

opens at steps or feed throughs

The other two conditions associated with multi-level metallization are high sheet resistance of metal and excessive leakage currents. These can be detected when their magnitude substantially increased the amount of infrared radiation emitted at those points where they occur.

2.4 Bond and Connections

Certainly the best way to pinpoint open wire bonds and high resistance wire bonds is through electrical resistance measurements. However this is an "after the fact" test, so that rework is necessary to correct the defective condition. A better approach that is now available through infrared techniques is real time monitoring and control of the bonding operation, so as to prevent poor bonds from occurring. The Thermal Bond Monitor was designed and developed just for this type of application, and its use drastically reduces the incidence of poor quality wire bonds.

2.5 Package

Package hermeticity is an item of paramount importance. However, unless the lid-sealing process involves welding or

high temperature bonding processes, infrared techniques will not be able to offer any advantage versus present conventional techniques. In cases where lids were spot-welded in place, then the Thermal Bond Monitor should be able to control the process so that the quality of the weld be kept within optimum control limits.

2.6 Photolithography and Diffusion

When these items are faulty, some elements of the integrated circuits incorporated in LSI devices will exhibit faulty performance. Therefore, their presence will be disclosed by the Semiconductor Junction Analyzer and also by the Fast Scan Infrared Microscope. In particular, defects such as current crowding and current voids in the junctions are detected through non-uniformity characteristics of the recombination radiation emitted by the affected areas. Photolithographic defects can be detected if they block some of the infrared radiation emitted by elements of the integrated circuits. However, detection of these photolithographic defects should be easier in most of the instances by using conventional visual inspection techniques.

2.7 Chip Mechanical

Again here visual techniques should enable the inspector to detect most of the mechanical defects affecting the

semiconductor chip or wafer.

2.8 Chip Mount

This appears to be a typical application for infrared techniques, since voids and discontinuities between substrate and the semiconductor chip or wafer appear in the infrared picture as areas where the heat transmission is impaired.

3. PROGRAM OUTLINE

In view of the above, it was decided to concentrate the effort of the present contract on the following applications which appear to hold the most promising potential for improving the LSI reliability:

3.1 Establishing the capability to detect electrical power dissipation anomalies, due to any of the several possible causes as discussed in Items 2.1 to 2.8; the instrument best qualified for this work is NASA's Fast Scan Infrared Microscope.

3.2 Establishing the capability to detect anomalies in the current flow through the junctions, due to incorrect doping, impurities, surface effects, etc.; the only instrument capable of yielding information of this nature is the Semiconductor Junction Analyzer.

3.3 Establishing the capability to control the quality of the wire bonds during bonding operation. The instrument to be used for this application is the Thermal Bond Monitor.

3.4 Establishing the capability to assess the quality of the wafer-substrate bond, including the identification of the location of the defects and their magnitude. The instrument to be used for this application is the INSPECT System.

3.5 Based on the above premises, a work program was drawn in which the sequence of operations was planned in accord with the availability of test equipment and of test specimens to be used. In particular, the following elements were deemed essential for the success of the program:

a. support by a complementary contractor, active in LSI production;

b. timely availability of semiconductor targets

c. timely availability of infrared test equipment

d. timely availability of thermocompression bonding equipment (chip bonders and wire bonders)

3.6 The work program is shown in Figure 2. This chart shows how the program was actually run, within the constraints of equipment and materials availability.

3.6.1 Specifically, work was first applied to develop thermal maps of single-metallization-layer integrated circuits of a type widely used in the LSI devices to be investigated in the present contract. Conspicuous anomalies were apparent between the infrared profiles of good and faulty units. Additional verification work was carried out later on.

3.6.2 Bond quality between LSI wafer and substrate was investigated as a function of heat transmission between said two elements. In correspondence of voids

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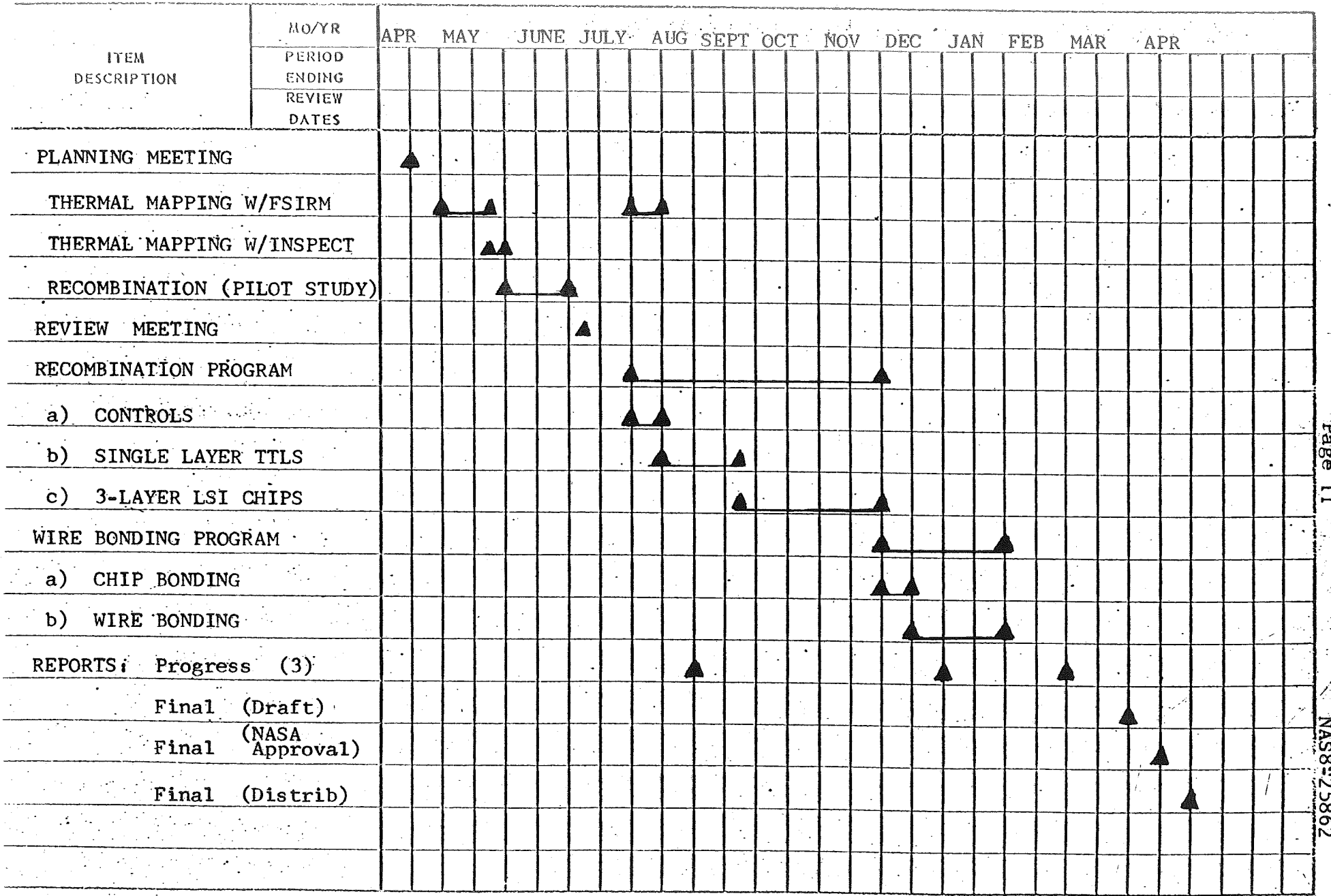
FIGURE 2.

RESPONSIBLE ENGR _____ UNIT _____ PROJECT _____ D.O. NO. _____



SYMBOLS: Δ——Δ = SCHEDULE LINE ○ = ACTUAL START

the infrared anomalies were quite noticeable.

3.6.3 A pilot study carried out on some single-metallization layer integrated circuits of the type described under 3.6.1 verified the feasibility of measuring the recombination radiation emitted by individual junctions of transistors operating in the integrated circuits.

3.6.4 On the basis of these findings, the Recombination Radiation Program subsequently described under Section 9 was planned in detail, in a review meeting held on July 8, 1970, between NASA, Texas Instruments and the Contractor.

3.6.5 The Recombination Radiation Program consisted of three phases:

a) establishing radiation standards with the help of simple control units;

b) measuring radiation levels on single-metallization layer units;

c) measuring radiation levels on three-metallization layer LSI chips.

3.6.6 Finally, the wire bonding control program consisted of two phases:

a) preparation of semiconductor chips bonded to their substrate with eutectic bonds of different,

but known, quality;

b) performing wire bonds on said chips under real-time control of the operation.

3.6.7 Interim Reports, classified as Phase A, B, and C, and a Final Report were planned in accord with the program outline.

4. COMPLEMENTARY CONTRACTOR

The technical support required for the conduct of this program consisted of the following:

a) supply bonding equipment;

b) supply semiconductors to be used as targets;

c) assist and advise in the conduct of the work.

Texas Instruments Co. was chosen by NASA to perform the above-mentioned tasks, under a separate contract designed to complement the one issued to Vanzetti.

5. TARGETS

The targets to be used in the course of this program were the following:

a) conventional integrated circuits, as basic calibration and reference items;

b) single-metallization layer integrated circuits, as intermediate reference elements and also for the wire bond monitoring program;

c) three-level metallization LSI circuits as final evaluation targets.

5.1 The devices mentioned under a) are simple integrated circuits, Type MC355, made by Motorola, and already used at Vanzetti's as a reference infrared radiation source. The unit is an array of five transistors, laid out on a silicon chip in a single metallization layer, with separate outside connections allowing for independent electrical energization of each transistor. Figure 3 shows the visible picture of one of these units, and Figure 4 shows its electrical schematic. The chip's surface is protected by a single layer of silicon oxide of unknown thickness.

5.2 The devices mentioned under b) are TTL (Transistor-Transistor-Logic) integrated circuits, quadruple 2-input NAND gates, made by Texas Instruments and designated as Type SN5400J. Figure 5 shows the visible picture of one

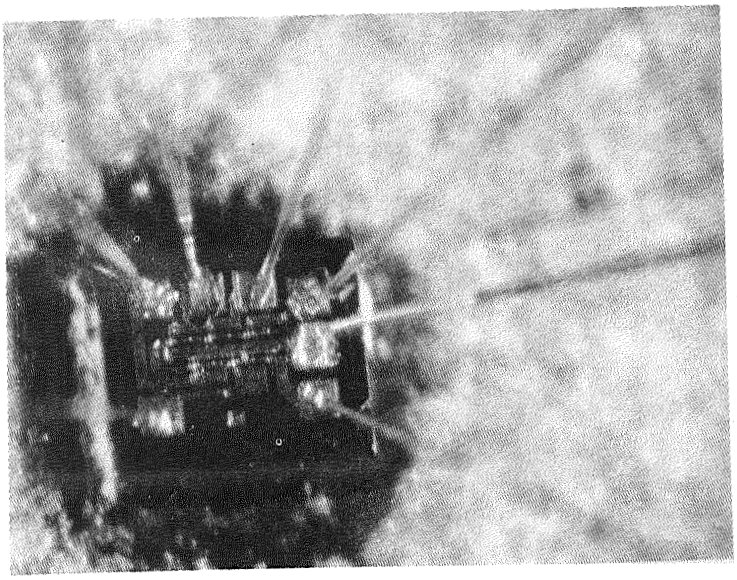


FIGURE 3. MC 355 IC (100 X)

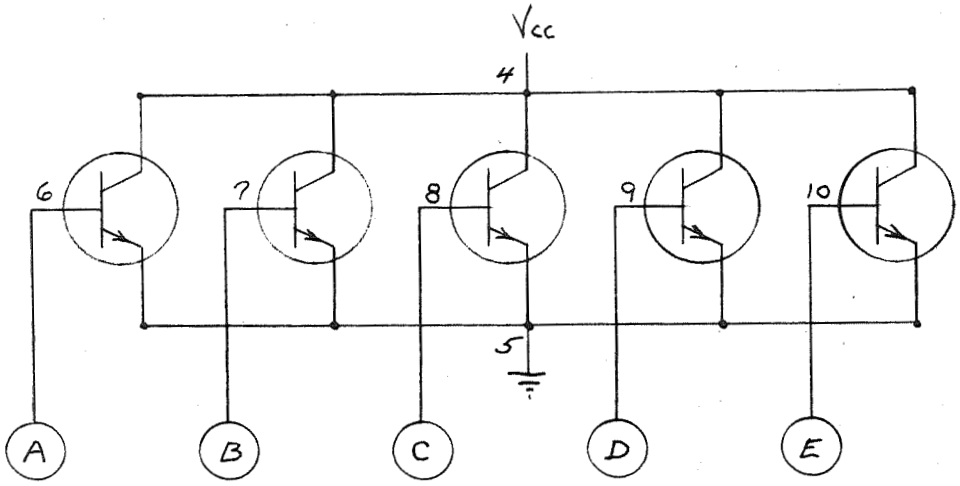


FIGURE 4. MC 355 IC Schematic

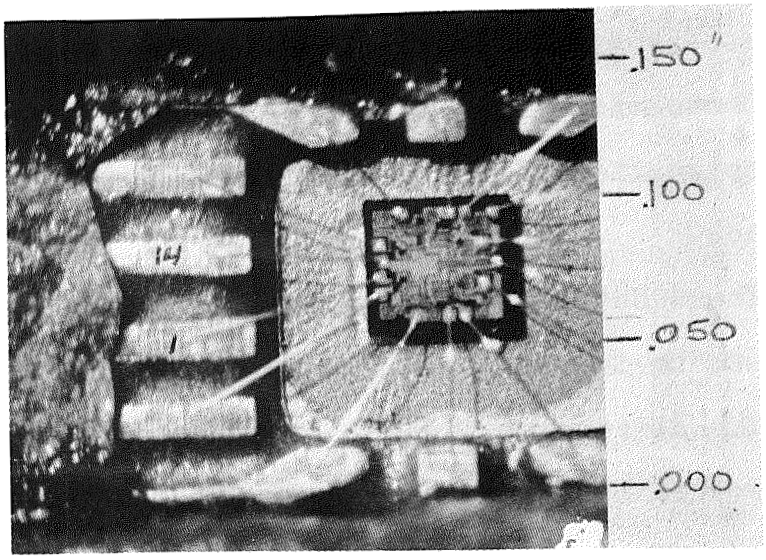


FIGURE 5. SN5400J

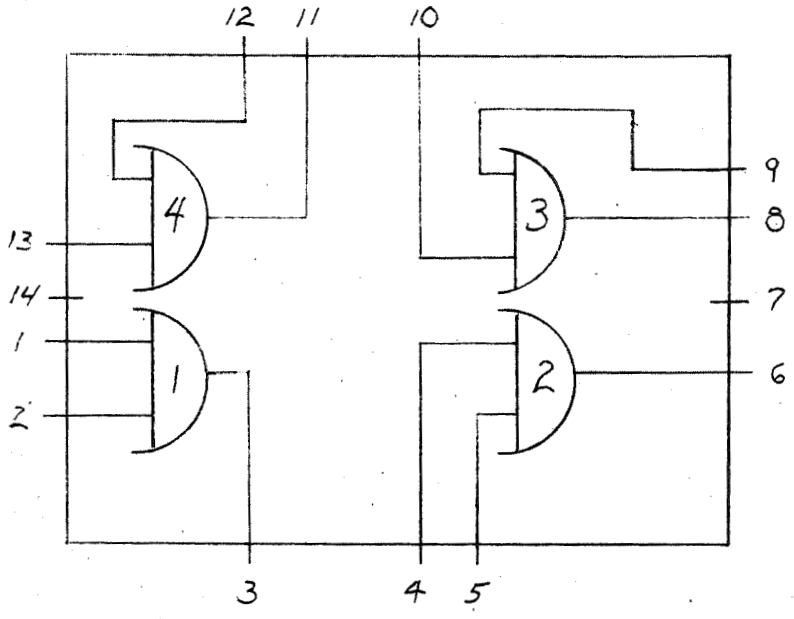


FIGURE 6. SN5400J

of these units, and Figure 6 shows the gates' configuration and their outside connections. The electrical schematic of one of these gates is shown in Figure 7, while Figure 8 is a photo-micrograph of one of these ICs, complete with the designation of the several elements of which it is composed.

These devices are typical of the ICs used in the LSI units to be investigated under this contract. However, the main difference lies in the fact that the TTL devices are covered by only one silicon oxide layer for protection purposes.

5.3 Most of the devices mentioned under c) are small fragments cut off complete LSI devices. They contain the same circuit described under 5.2. However, these units have three metallization layers, separated by silicon oxide layers, so that a certain amount of attenuation of the recombination radiation signal emitted by the junction is to be expected.

These fragments are of irregular shape and size, and one of them is shown in Figure 9. Custom-made wire bonds connect inputs and outputs to the outside terminations of the header to which the chips are eutectic-bonded.

5.3.1 Included under c) are also some LSI wafers, either bonded or not bonded to a substrate. These units were to be used to evaluate the capability of detecting hidden bond defects.

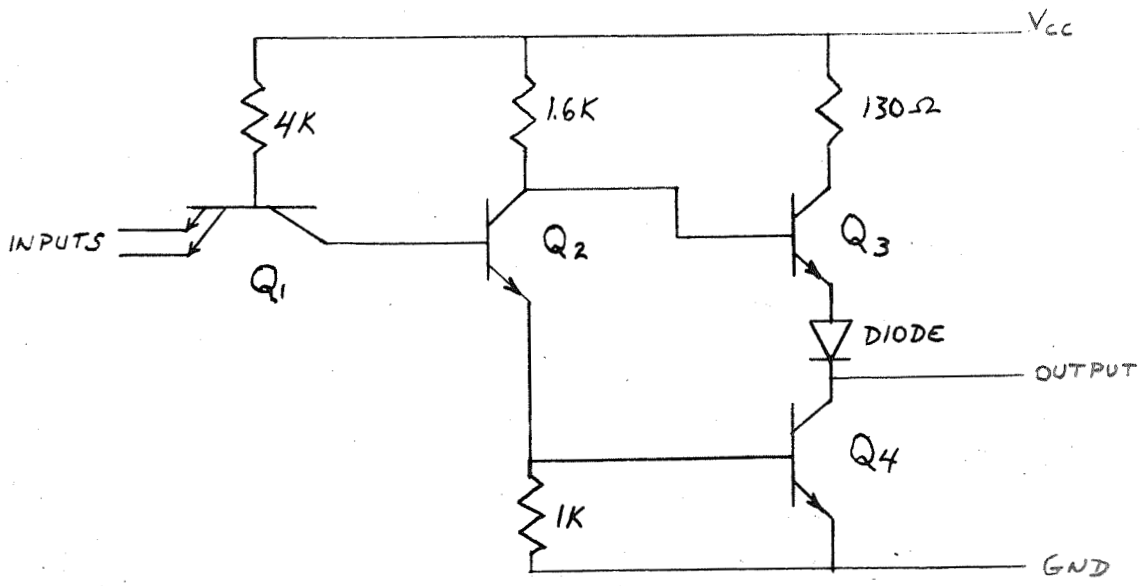


FIGURE 7. SN5400J (Single gate schematic)

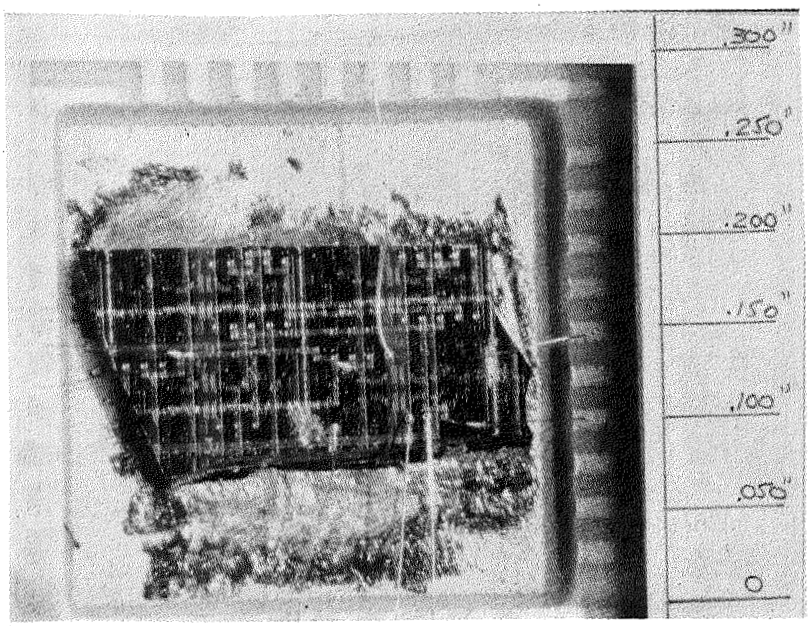


FIGURE 9. LSI Special Unit #2
(15X magnification)

FIG. 8
SN 5400 J DEVICE (CHIP PHOTOMICROGRAPH)

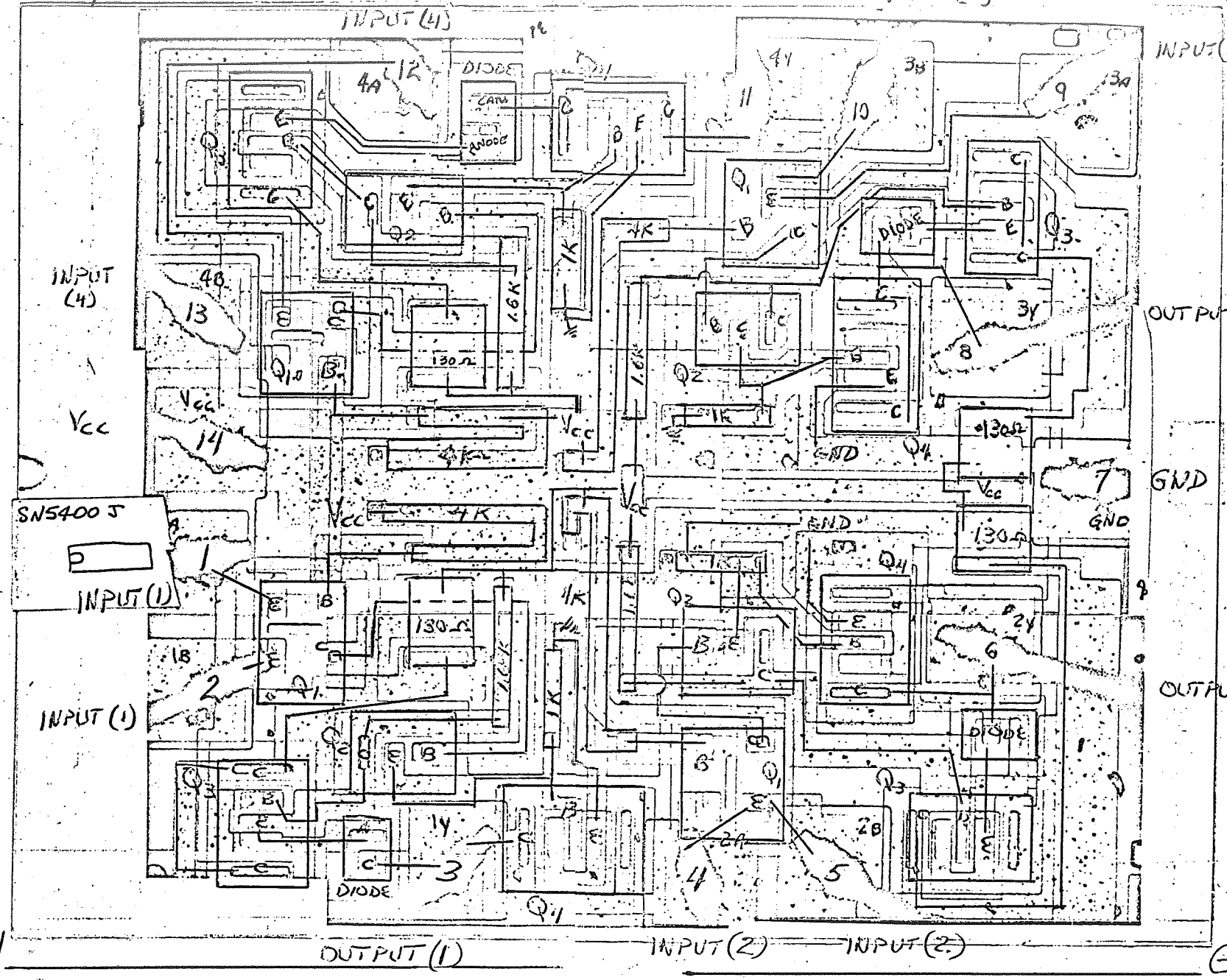


FIG. 8

6. THE TEST EQUIPMENT

The infrared test equipment to be used in the course of this program is the following:

6.1 The NASA Fast Scan Infrared Microscope (Figure 10) is an instrument which senses the heat radiated from semiconductor devices as electrical energy is dissipated by the discrete active elements incorporated in the device. The instrument processes the collected radiation and displays it in two ways: as an analog profile for each scan line, on an oscilloscope; and as a thermal map of the device under test on memory scope. The thermal map is made up of dots representing the points at which the analog signal supplied by the detector crosses the thresholds that have been pre-set at the outset. A range of 1 to 15 thresholds is possible. The microscope has an area resolution of .003", temperature resolution of $4^{o}C$ at $60^{o}C$ and $2^{o}C$ at $100^{o}C$, a typical scan speed of 25 lines/second and it accepts a target 0.080" x 0.080" as maximum size.

6.2 The Barnes Infrared Microscope (Figure 11) is a point-detecting instrument that supplies temperature information on the basis of the infrared radiation emitted by the target. Scanning is done manually with a micrometric substage. It has an area resolution of 0.0028" at 150X

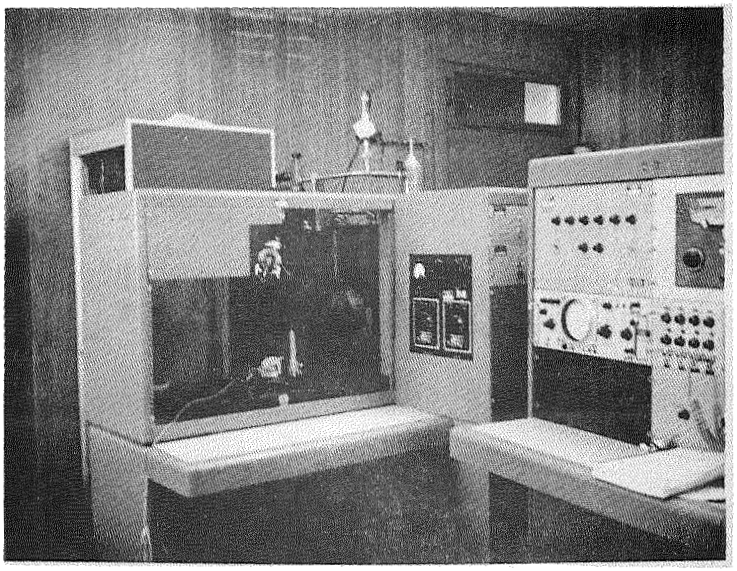


FIGURE 10. NASA Fast Scan IR Microscope

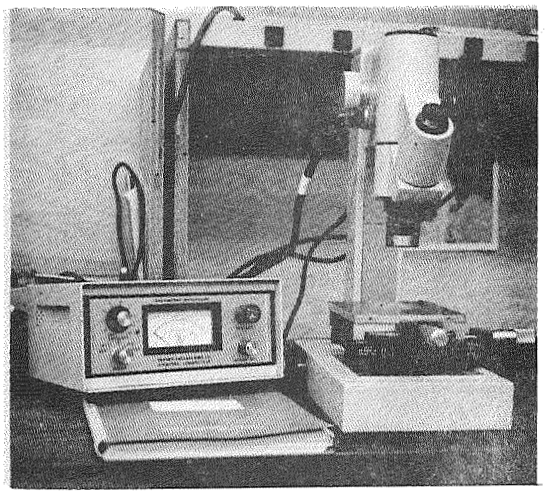


FIGURE 11. Barnes Infrared Microscope

magnification, and a thermal range of 165°C above ambient, for a target having blackbody emissivity. A special control, located on the panel of the display console, provides compensation capability for targets having different emissivity.

6.3 The INSPECT SYSTEM (Figure 12) is an infrared scanner which senses the heat radiated from electronic components as electrical power is dissipated by each of them. The instrument processes the detected signal and displays it, line by line, as an analog profile, on an oscilloscope. Also, it converts this information into digital data which is printed out by a teletype. It covers a range to 300°C above ambient, has a thermal resolution of ±0.1°C at blackbody emissivity, a spot-size of 0.020" and a system spatial resolution of 0.050". The scanning elements are run by a computer and its memory can hold all the information related to as many as 256 points or elements of the target.

6.4 The Thermal Bond Monitor (Figure 13) is an infrared detection system which continuously measures, in real-time and without physical contact, the infrared radiation emitted by a semiconductor chip during bonding to the substrate. The system can also be adapted to monitor other type bonds. It has a temperature range of 200° to 1000°C at blackbody emissivity, an accuracy of ±1% of reading and a 1 millisecond detector response. Its main feature is the use of a single

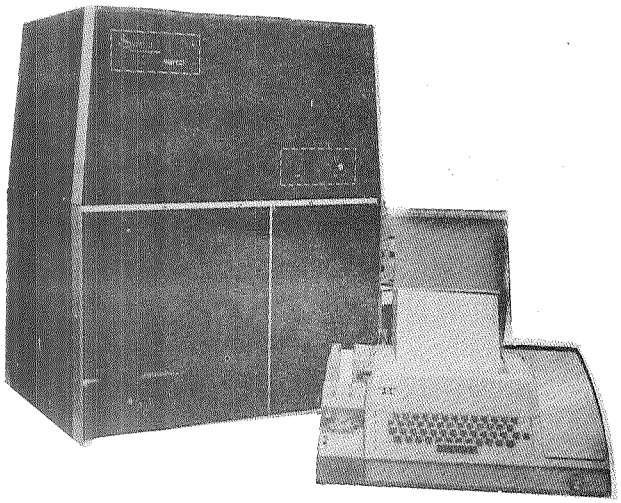


FIGURE 12.
The INSPECT System

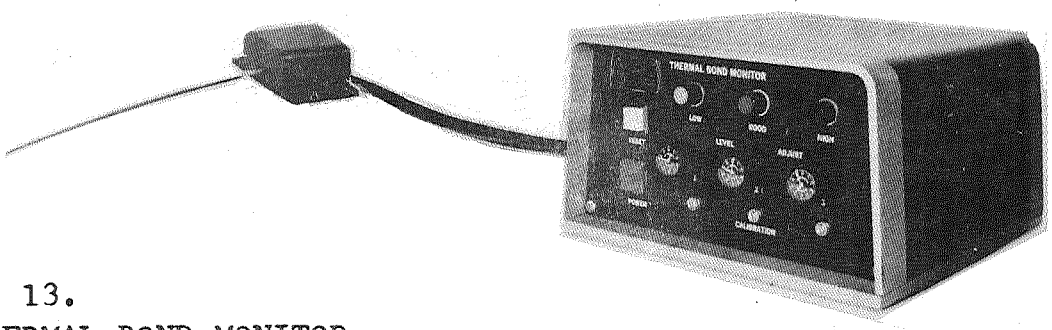


FIGURE 13.
The THERMAL BOND MONITOR

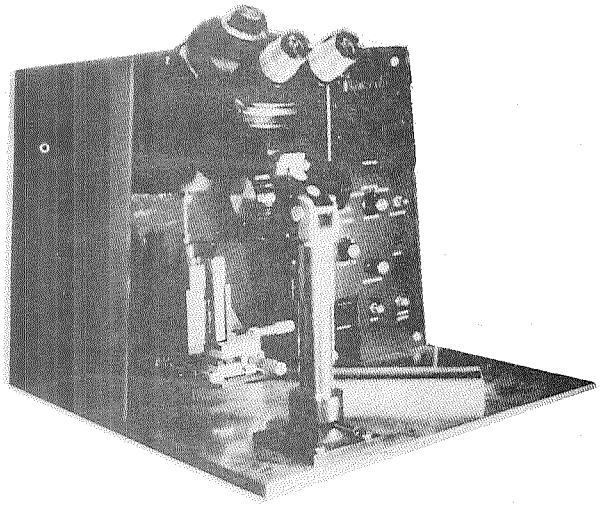


FIGURE 14.
The SEMICONDUCTOR JUNCTION ANALYZER

optical fiber, typically 14" long and 0.006" in diameter, which allows the detector to "see" the target (e.g. a semiconductor chip) even when it is hidden from direct view. Temperature display is obtained through three adjustable thresholds, that can be set at any desired temperature level. Temperature measurement can be obtained by reading the amplitude of the output signal on an oscilloscope that can be connected to the instrument.

6.5 The Semiconductor Junction Analyzer (Figure 14) is an infrared detection instrument which measures the recombination radiation emitted by silicon semiconductor junctions at 1.1 microns wavelength.

Principle of Operation - Recombination radiation is the energy released by current carriers (electrons) when they recombine with "holes". This energy is generated as photons when electrons make the transition from the conduction band to the valence band. The greater the current flow through the junction, the greater the number of electrons and the greater the recombination power released at transition. Consequently, an infrared detector can measure the current flow as a function of the radiation emitted by a junction. The detector of the Semiconductor Junction Analyzer can view a junction by using optical fibers of diameters between 0.002 and 0.040 inches. This provides the capability

to map junctions or chips with any desired degree of spatial resolution. This approach further makes possible electrical studies of chips or circuits using no physical contact with the items under study.

The signal from the detector is amplified and treated to eliminate noise. The output is displayed on a Digital Panel Meter (DPM) as a decimal number to indicate recombination radiation power. The detector covers a spectral range from .4 to 1.2 microns at 10% power points, has a sensitivity of 1.40×10^{8} volts/watt of infrared energy at 1.0 microns, a time response of 4 to 20 seconds over 5 ranges of time constant, and an accuracy of $\pm$5% of full scale.

6.6 Miscellaneous equipment was used in order to energize the TTL test device, to collect the data in the form of Polaroid pictures of oscilloscope displays, and to position the test devices in the focal planes for optimum test results.

7. THE THERMOCOMPRESSION BONDERS

In order to carry out the last part of the program, two pieces of manufacturing equipment were needed:

a) a die-attach machine

b) a wire bonder

7.1 The die-attach machine available at the Vanzetti Laboratory is a thermocompression chip bonder, Model 642, made by Kulicke & Soffa. (See Figure 15). It performs eutectic bonding of semiconductor chips by heating the substrate and "scrubbing" against it the chip, which is held by vacuum suction at the tip of an unheated steel collet. For silicon chip on a gold substrate, the eutectic flows at 375°C.

7.2 The wire bonding machine is shown in Figure 16. It is a model made by Texas Instruments and extensively used for their manufacturing operation. It requires a substage kept at 290°C and a collet heated at 180°C. The gold wire used to make wire bonds with this machine was 0.0007".

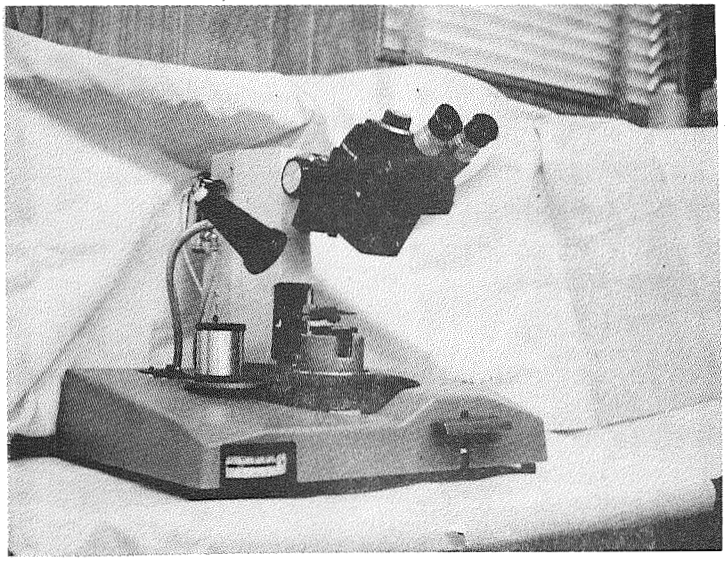


FIGURE 15. K & S Model 642 Die Attach Machine

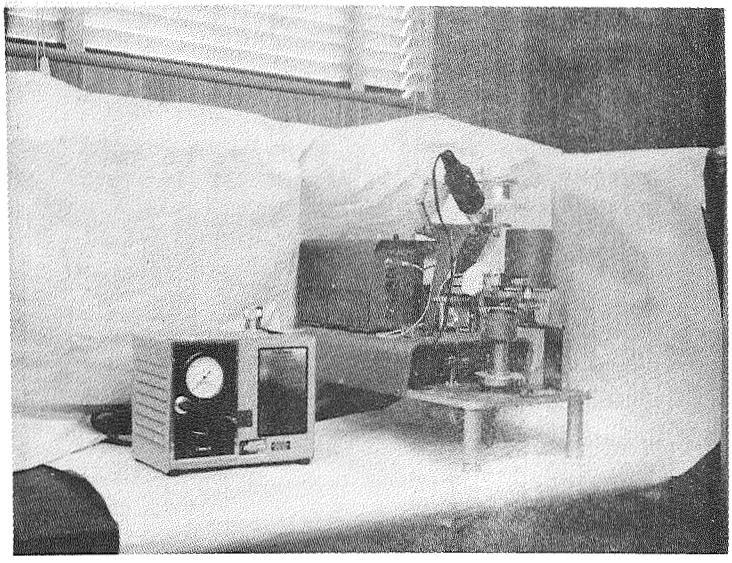


FIGURE 16. T. I. Wire Bonding Machine

8. THERMAL MAPPING

This program was designed to measure, in location and magnitude, the temperature differentials generated in the targets when these are thermally energized.

Thermal energization can be obtained either from within (e.g. by electrical power dissipation) or from without (e.g. by heat injection). Both methods were used in the course of this program, as described below.

8.1 The NASA Fast Scan Infrared Microscope was used to scan electrically energized TTL devices, in order to obtain thermal maps that may be used as standard against which to compare the same circuit types contained on an LSI device wafer.

A thermal map will show temperature variations on the test device as a function of component location, amount of wattage dissipated, and thermal conductivity of the materials. For this test an electrical energization mode was chosen (Figure 17) to scan the device in a dynamic mode. To evaluate the effect of the dissipation of each gate, devices were chosen that had inoperative gates as well as operative gates.

Thermal maps of three devices were recorded, of which Figure 18a is representative. This device (#6) had gate #4 inoperative. This map is correlated with a device photo

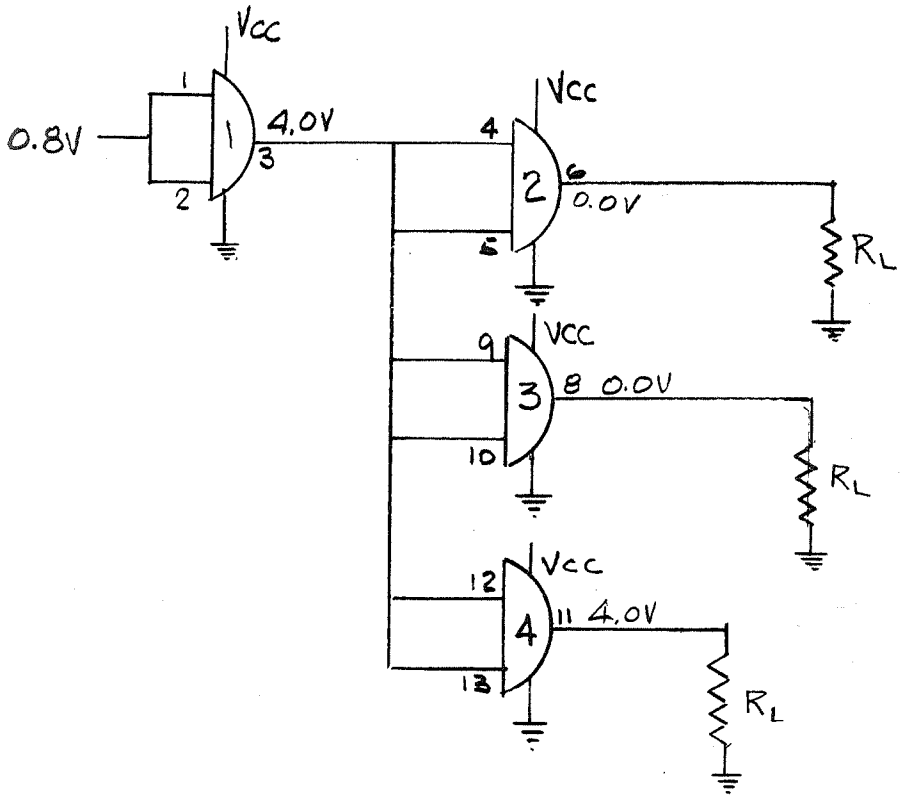


FIGURE 17. Electrical Energization of TTL Device

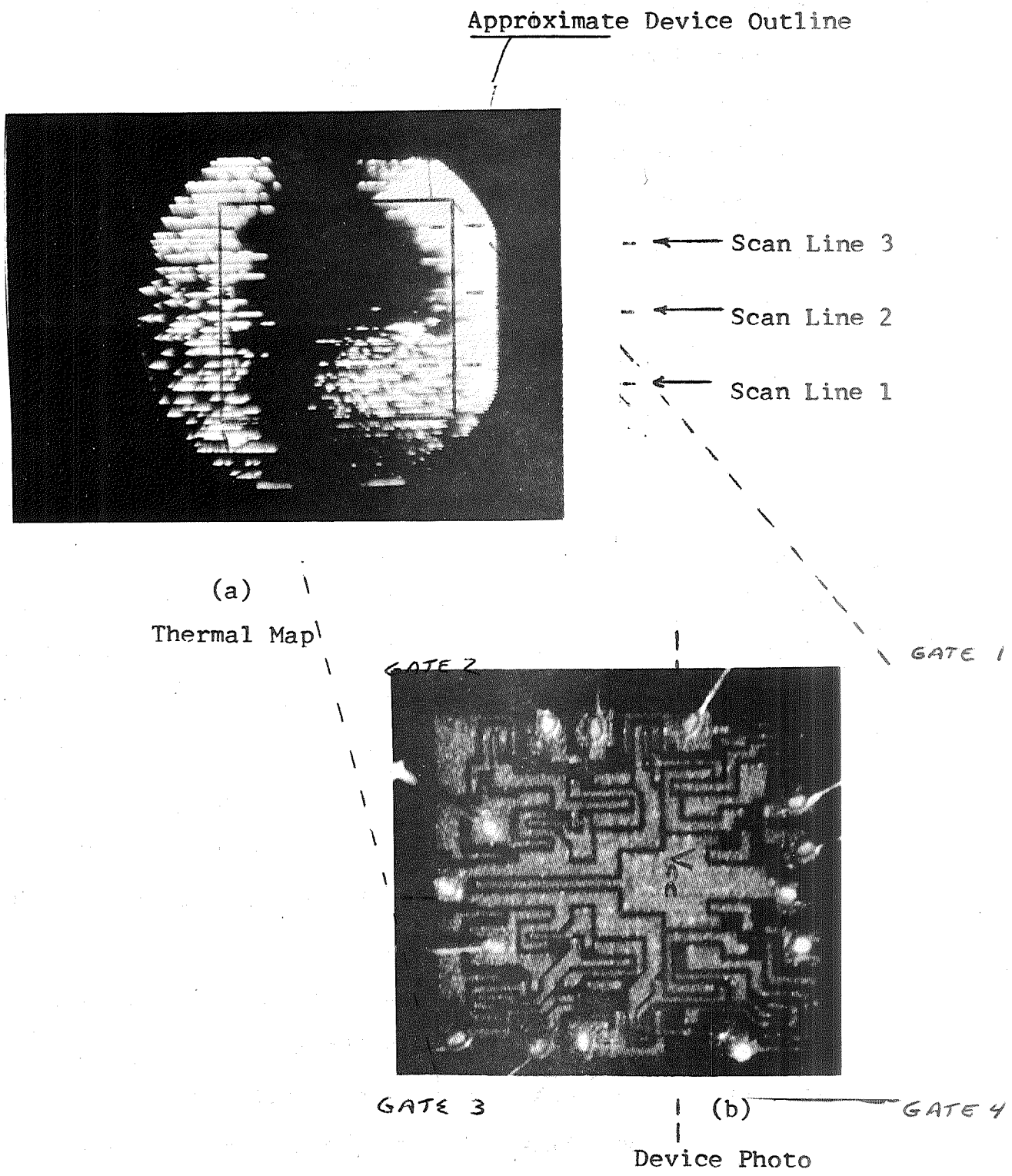


FIGURE 18. Thermal Map of TTL Device (a & b)

(Figure 18b), showing device size and the orientation of the device relative to the oscilloscope display. Also shown are three single line scans (Figure 18c) showing temperatures across the device.

Figure 18c shows three oscilloscope traces representing the thermal profiles across the device, shown as scan lines 1, 2 and 3 on Figure 18a. In this display the direction of the scan line is from right to left. In scan line 1 we see the signal rising through the thresholds, generating the dense white area on the right. As the signal peaks and crosses the top threshold many times, due to the lower temperature of gate #4, we see in Figure 18a the white area at the lower right, which indicates lack of electrical power dissipation in correspondence of gate #4. As the scan proceeds, the signal rises above the top threshold, generating a dark area in the left lower corner of the device, corresponding to gate #3. Beyond the edge of the chip, the signal drops at a lower rate than the original rise, generating a white area on the left, although less dense due to the slower drop in temperature.

Scan lines 2 & 3 can be analyzed in the same manner; here the signal remained above the top threshold longer in each case, resulting in wider dark areas corresponding to the warmer temperatures present in the areas of gates #1 and #4, both dissipating electrical power.

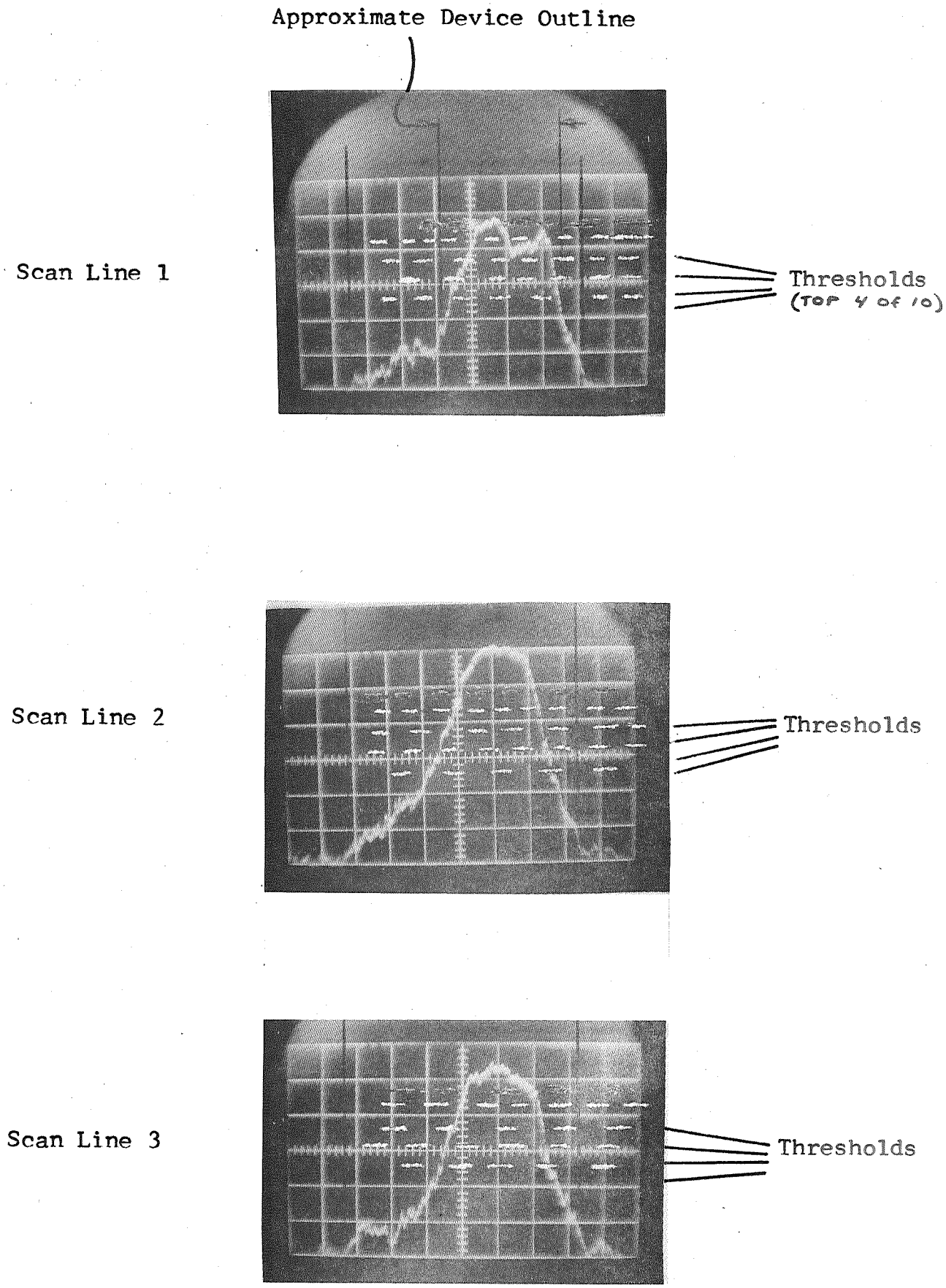


FIGURE 18. Thermal Map of TTL Device (c)

The traces of Figure 18c show how differences in surface temperatures of TTL circuits are detected and displayed by the Fast Scan Infrared Microscope. It is in this way that manufacturing or workmanship defects, accompanied by changes in power dissipation, can be pinpointed in ICs, no matter whether they are discrete or incorporated in LSI circuits.

Analysis of Figure 8 and Figure 18a and 18b shows that, in gates #1 and #4, most dissipative components are connected by metallization marked Vcc; thus, this area will tend to be warmer, along with the dissipative components themselves, than the remainder of the device, and this is borne out in Figure 18. The thermal map dark areas within the device outline are warmer areas as subsequently verified by the Barnes Microscope. (See following section).

8.2 The Barnes Infrared Microscope was used to verify the data from the NASA Fast Scan Infrared Microscope. Measurements were made by mounting the device in an appropriate holder, energizing it in the configuration shown in Figure 17, scanning it manually with the micrometer substage, and reading the device temperature in areas where the NASA Fast Scan Infrared Microscope indicated there were differences. The largest Δt increment found on the device was 3^{o} - $4^{o}C$ in the area of Vcc metallization connections to dissipative components.

8.3 The INSPECT System was also tried in the task of detecting thermal anomalies in TTL devices affected by

faulty operation. The INSPECT System's thermal profile display of a device under test is rather simple and easy to interpret. It is the presentation of infrared radiation emitted by all the points along a single line scan traversing the device under test, and it shows very plainly, within the resolution of the system, the peaks and valleys of high and low temperatures located along the scan line. In order to evaluate the detectability of electrical defects showing up as temperature variations due to differences in electrical power dissipation, a test was conducted as follows: the thermal profile of a TTL device, 100% operative, was compared to the thermal profile of another TTL device having one defective gate, (fault unknown) and three operating gates. The test circuit schematic is shown in Figure 19.

The two sets of thermal profiles of two TTL devices, one of which is good and the other defective, (Figures 20 to 23) are indicative of the temperature evaluation that can be made of devices operating in the same electrical energization mode, but having different internal circuit conditions resulting in different amounts of power dissipation. In the illustrations the oscilloscope traces show the time sequence increase in temperature of the TTL device and package due to power dissipation in the device. Device #5 profiles show the effect of the defective gate, in the faster rise of the temperature as compared with the

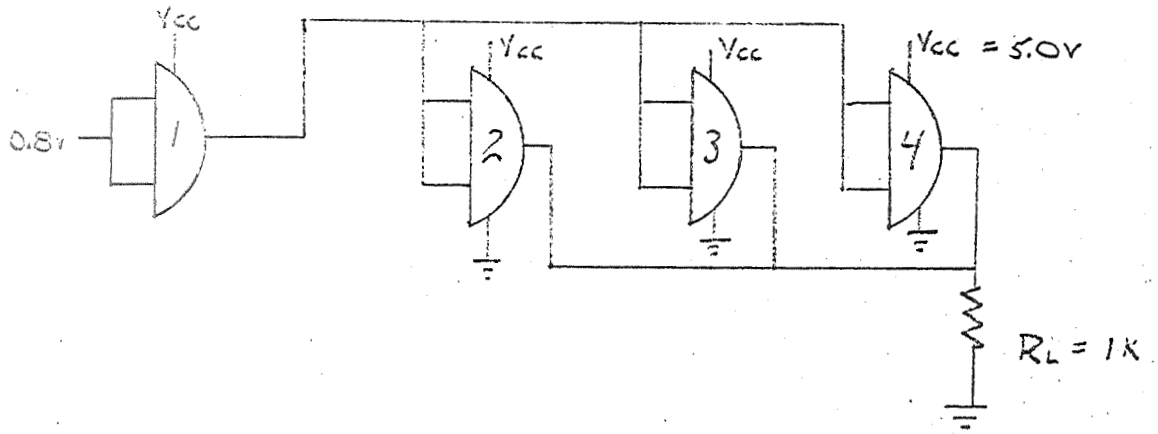
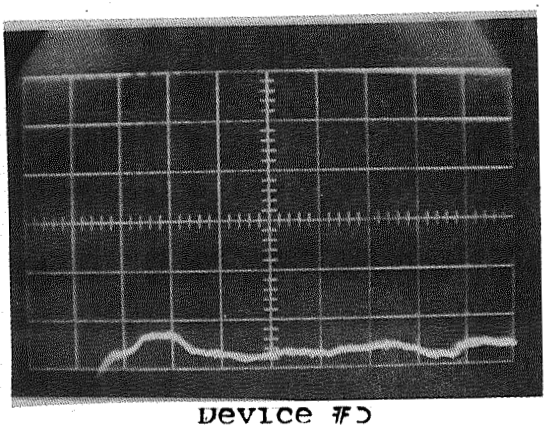
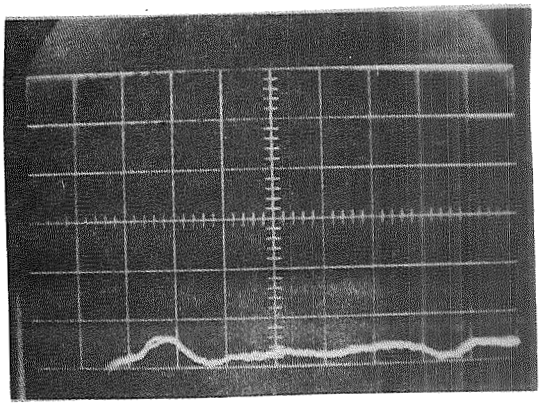


FIGURE 19. Electrical Energization of TTL Device for INSPECT Test

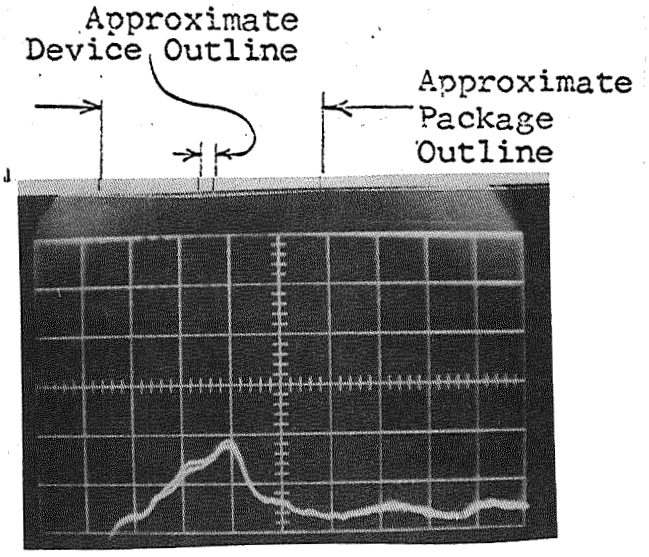


Device #5
1 Defective Gate

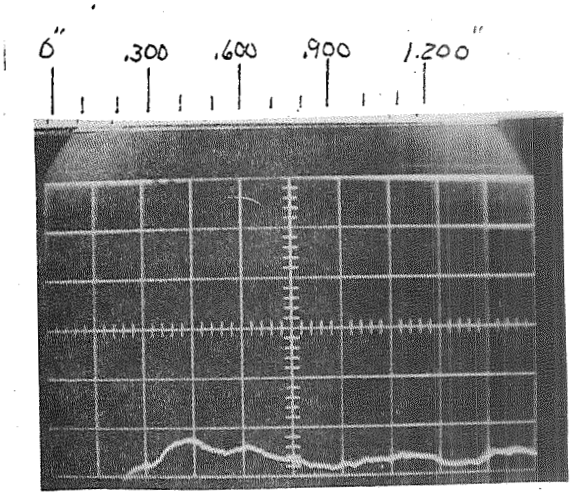


Device #2
All Good Gates

FIGURE 20. TTL Devices:
IR Profiles at Time 0

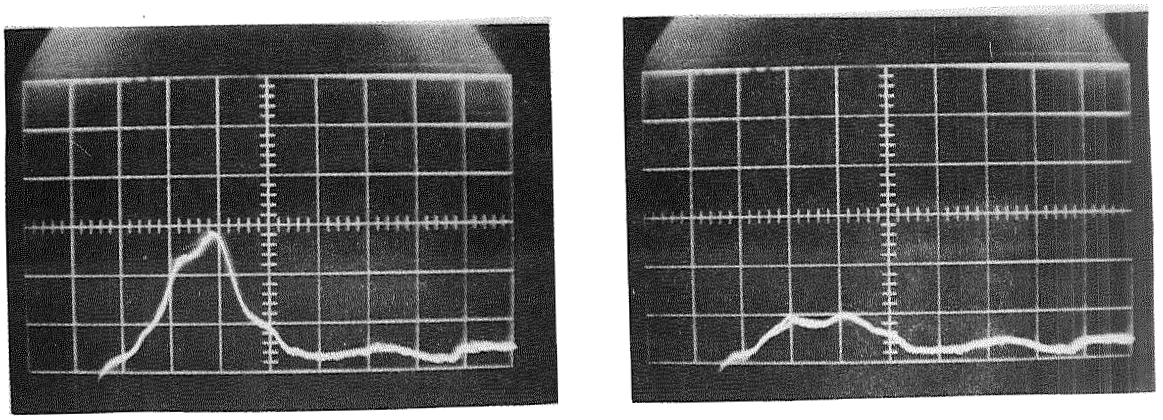


Device #5



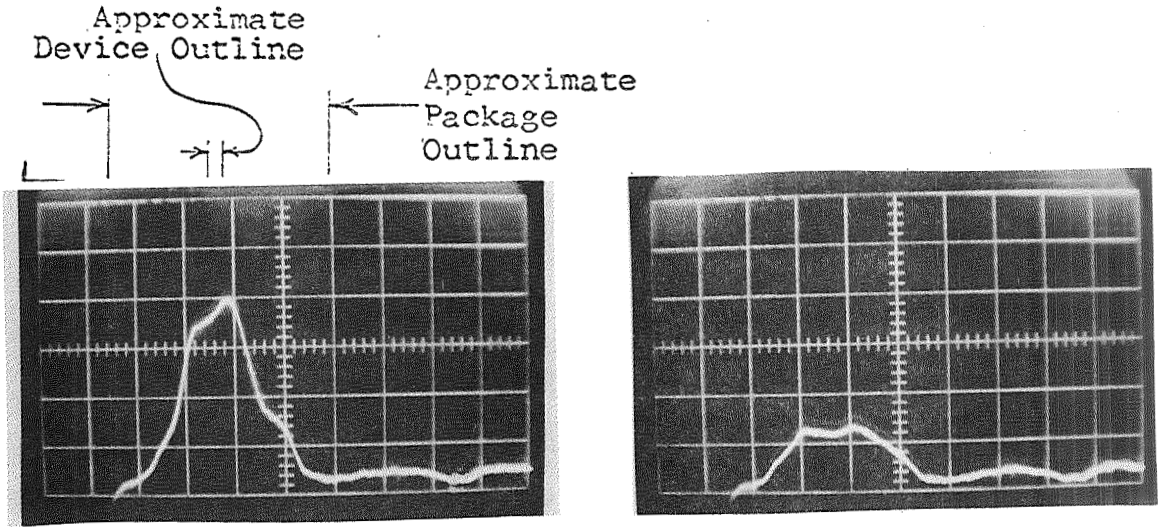
Device #2

FIGURE 21. TTL Devices:
IR Profiles After 10 Seconds
from Energization



Device #5 Device #2

FIGURE 22. TTL Devices: IR Profiles after 20 Seconds from Energization



Device #5 Device #2

FIGURE 23. TTL Devices: IR Profiles after 30 seconds from Energization

profiles of device #2, which is operating normally. Other faults could show up as higher or lower localized temperatures, depending upon the effect of faults causing power dissipation changes.

8.4 In order to evaluate the quality of LSI wafer to header bonds, a different test using the INSPECT System was made on a mechanical reject LSI having second layer metallization. The LSI wafer was attached to a heat sink with heat sinking compound, intentionally leaving a void. (Figure 24).

The heat sink, in turn, was mounted on a heat source, again with heat sink compound, and heated to a fixed temperature of 60°C.

Figure 25 shows the oscilloscope trace of the line scan passing through the points A and B that are the limits of the heat sink. We can see that in the area comprised between C and D (the LSI limits) the temperature falls very rapidly as the detector's point of view moves from the well-bonded area towards and onto the unbonded area. This thermal profile could be compared, in the reverse sense, to the thermal profile of an LSI device which is generating heat through electrical power dissipation. In actual operation, the device would run hotter where the void occurs.

The results, Figure 25, show that monitoring of wafer

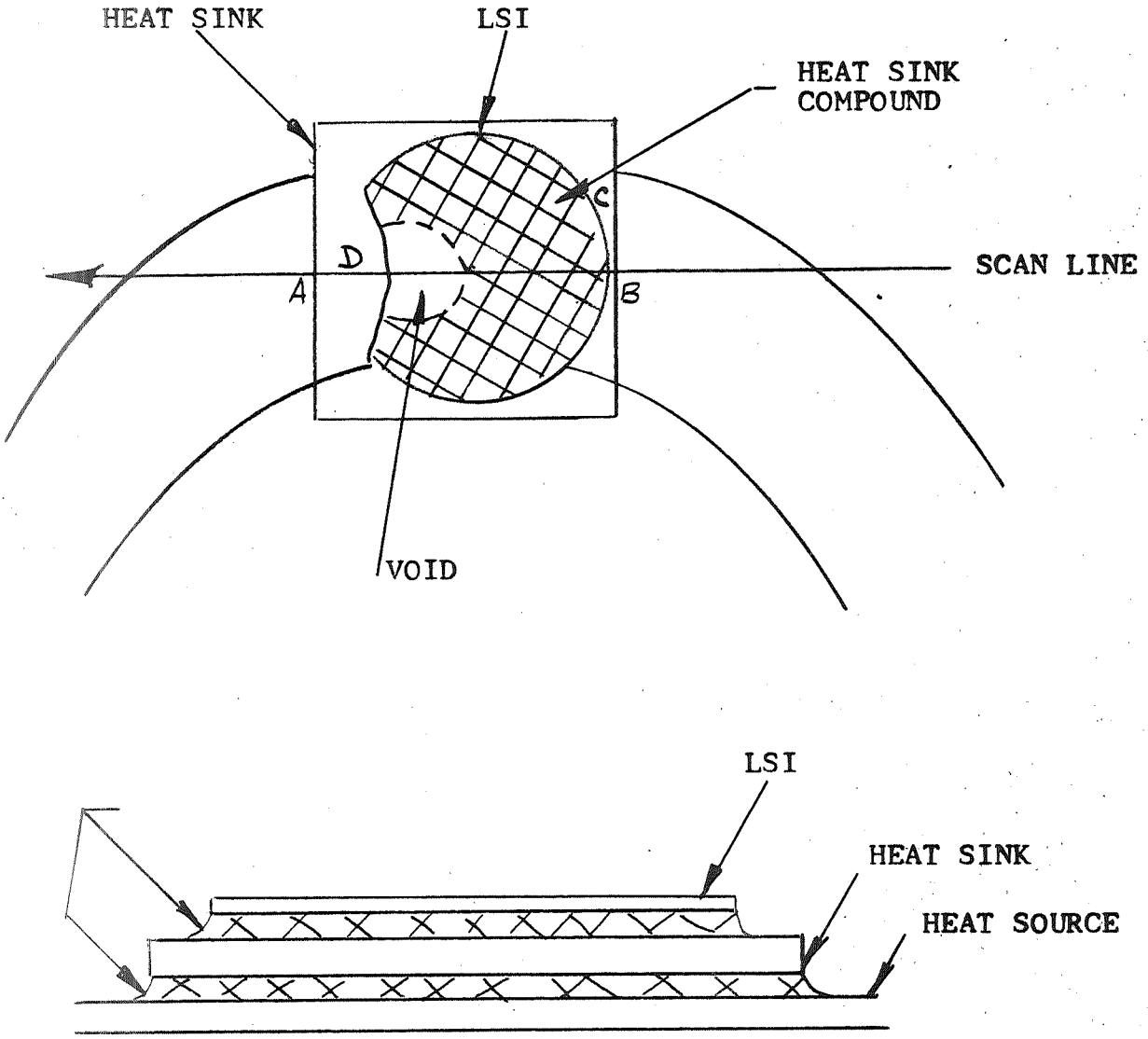
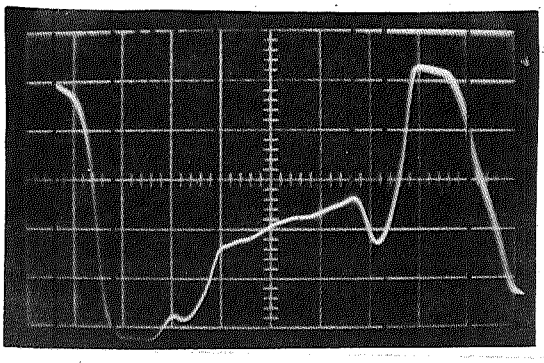
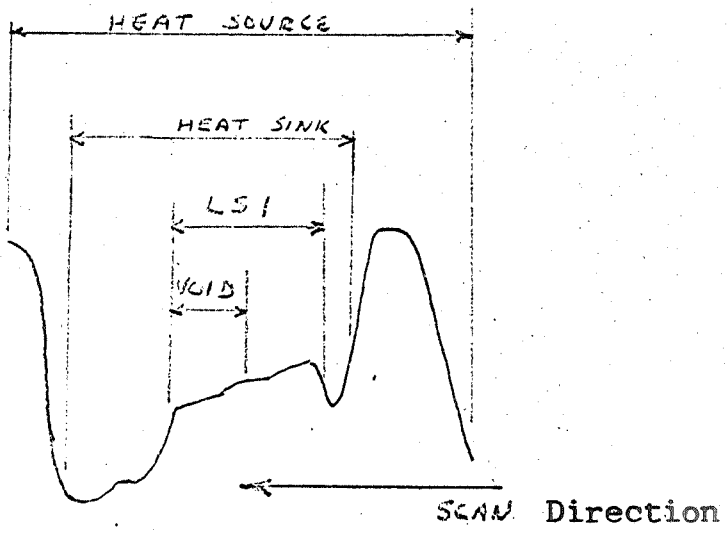


FIGURE 24. Wafer Bond Quality Evaluation



← Direction of Scan

Thermal Profile of Wafer Bond Test

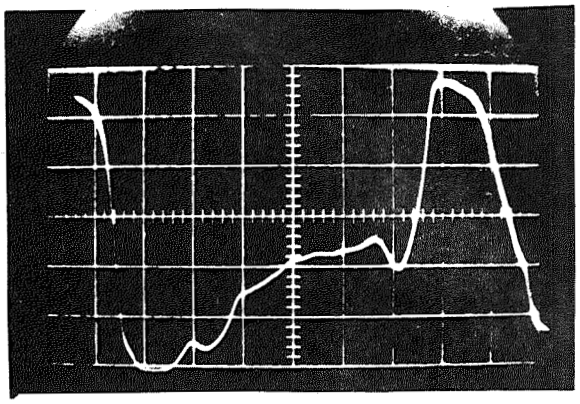


Analysis of Thermal Profile of Wafer Bond Test

FIGURE 25. INSPECT Scan Traces Across LSI Wafer for Bond Quality Evaluation

to header bonds, after the actual bond operation, can be performed reliably. To verify further the result of the test in Figure 25, the device was cooled very quickly by flooding with liquid nitrogen, while observing the thermal profile. The result, shown in Figure 26, is that the wafer temperature, in the void area only, decreases very quickly, accentuating the effect of the void in the wafer to header bond.

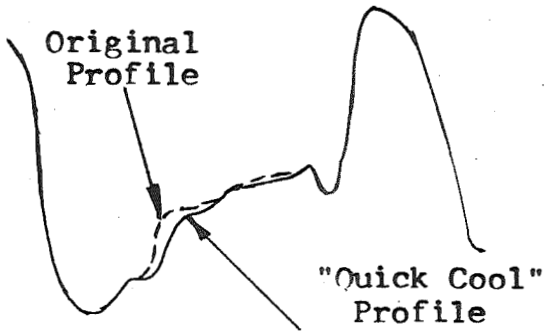
The result, Figure 26, illustrates how a void in the wafer to header bond shows up on the thermal profile. Conversely, in electrical operation the area located in correspondence of a bond void would show up as a positive peak.



← Direction of Scan

Thermal Profile of Wafer Bond Test

(Quick Cool Test)



← Direction of Scan

Comparison of Thermal Profiles of Wafer Bond Test

(Quick Cool Test)

FIGURE 26. INSPECT Scan Traces Across LSI Wafer During Quick Cool Test for Bond Quality Evaluation

9. RECOMBINATION RADIATION STUDY

As already discussed in 6.5, it is now possible to detect and measure the recombination radiation emitted by semiconductor junctions when electrical current flows through them. This is an infrared test that yields data quite different from the thermal radiation measurements described in Section 8. Up to this point, all the measurements taken were of incoherent radiation emitted by the semiconductor material; in this program, measurements were taken of the radiant energy emitted at a specific wavelength (coherent radiation), inherent to the energy levels defining the "forbidden gap" of the semiconductor material. In particular, silicon devices emit recombination radiation at a wavelength of 1.1 microns. Furthermore, the emission takes place only from the area of the junctions, as opposed to the thermal radiation, which is emitted by all points of the target's surface.

In practice, the measurement of recombination radiation is performed by electrically energizing the target, and visually (viewing it through a stereo microscope) aligning the junction of interest under the front end of an optical fiber whose output end faces a detector. In this way the radiant energy emitted by the junction is forwarded to the infrared detector. In turn, this detector converts the radiation into an electrical signal which is processed and displayed on a Digital Panel Meter

in millivolts, and is available for oscilloscope presentation or other signal analysis techniques. The alignment of the target with the optical fiber is done manually, using a micrometric multi-stage positioning substage having micrometer adjustments in the x, y and z directions.

9.1 Recombination Data of Control Units

As a first step, the Motorola ICs, type MC355, were used as control units in order to establish basic reference data against which to compare the readings of LSI-related units.

These devices were energized according to the test setup shown in Figure 27, and the following set of data were obtained and recorded as typical of these units:

(Data Taken with a .002" Diameter Optical Fiber)

Input Current (Ma)	Digital Meter (mv)
0	0-1 (drift)
2	0-2 (drift)
4	6
8	21
10	29
12	38
20	78
30	133
40	177
60	300

(Data Taken with a .006" diameter Optical Fiber)

Input Current (ma)	Digital Meter (mv)
0	0-1
2	3
4	20
8	63
10	96
12	120
20	235
30	397
40	538
60	907

This data has been plotted in the chart of Figure 28 and has been verified as consistent and repeatable.

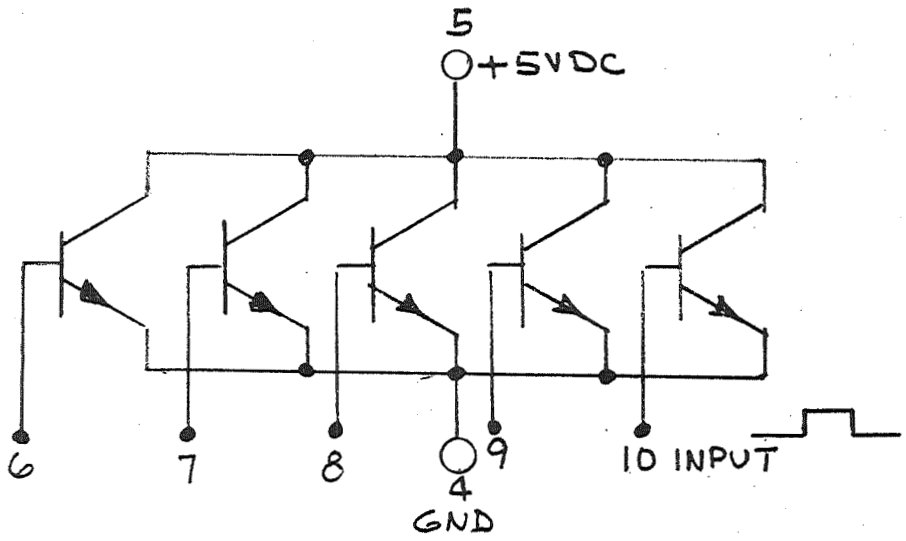
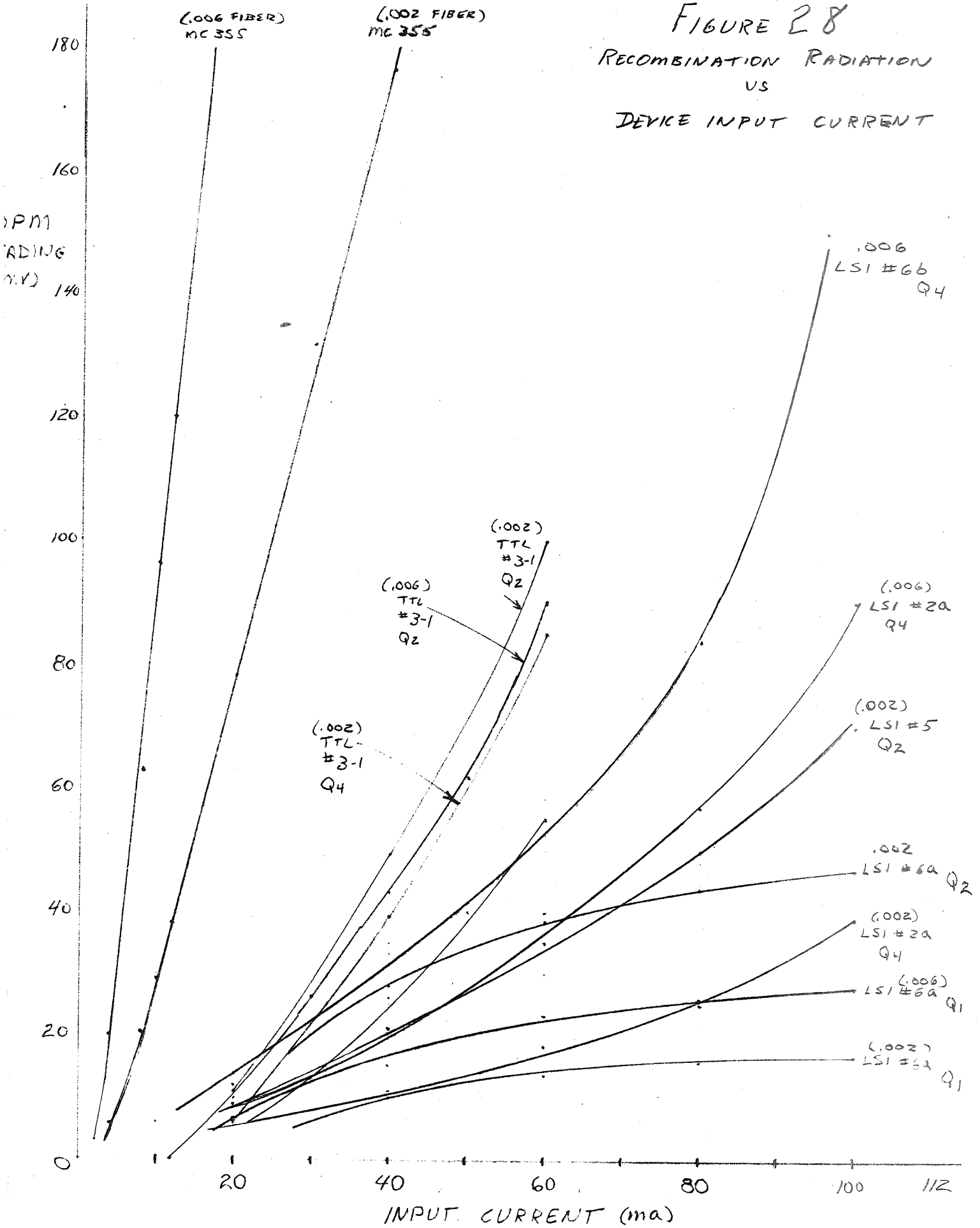


FIGURE 27. Test Setup of MC355 for Recombination Radiation Measurements

NAS8-25862

FIGURE 28

RECOMBINATION RADIATION
VS
DEVICE INPUT CURRENT



9.2 Recombination Data of TTL Devices

Recombination radiation measurements of these devices were performed as an intermediate step in the progression towards LSI performance testing.

These measurements were divided in two phases: Phase 1 was designed to verify the feasibility to detect recombination radiation from discrete junctions of electrically energized TTL devices, while Phase 2 was designed to obtain repeatable measurement data and to develop a correlation between radiation and current flow through the junctions.

9.2.1 Phase 1. Feasibility Program

Several TTL devices were energized, as in Figure 29, with an input pulse of 2.5v, 20μ seconds

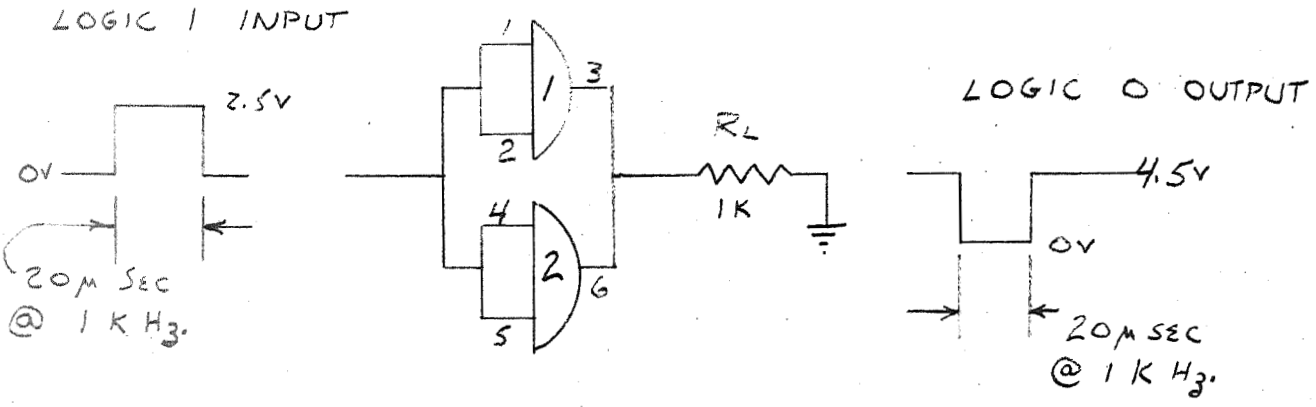


FIGURE 29. Test Setup of TTL Devices for Phase 1 Recombination Radiation Study

duration, and 1k Hz repetition rate. Only gates 1 & 2 were energized under the same electrical condition, while gates 3 and 4 were not operating. Purpose of this configuration was to ascertain whether differences in recombination radiation could be detected between active and non-active elements.

The recombination radiation map (Figure 30) that resulted indicates, when compared to the device map of Figure 31, that recombination radiation is detected in the area of transistor junctions. The magnitude of the signals detected has been recorded in millivolts from the DPM display, and it appears correlated with the magnitude of the current through the junctions. As can be seen, the output transistor Q4, which has the largest current flow when the device gate is in the logic 0 state, radiates higher recombination radiation power.

The levels of radiation measured are dependent: a) on the alignment and distance between the junction and the optical fiber; b) the amount of current flowing through the component (junction), and c) the fractions of the viewing area covered by opaque metallization that reduces the amount of the signal reaching the detector.

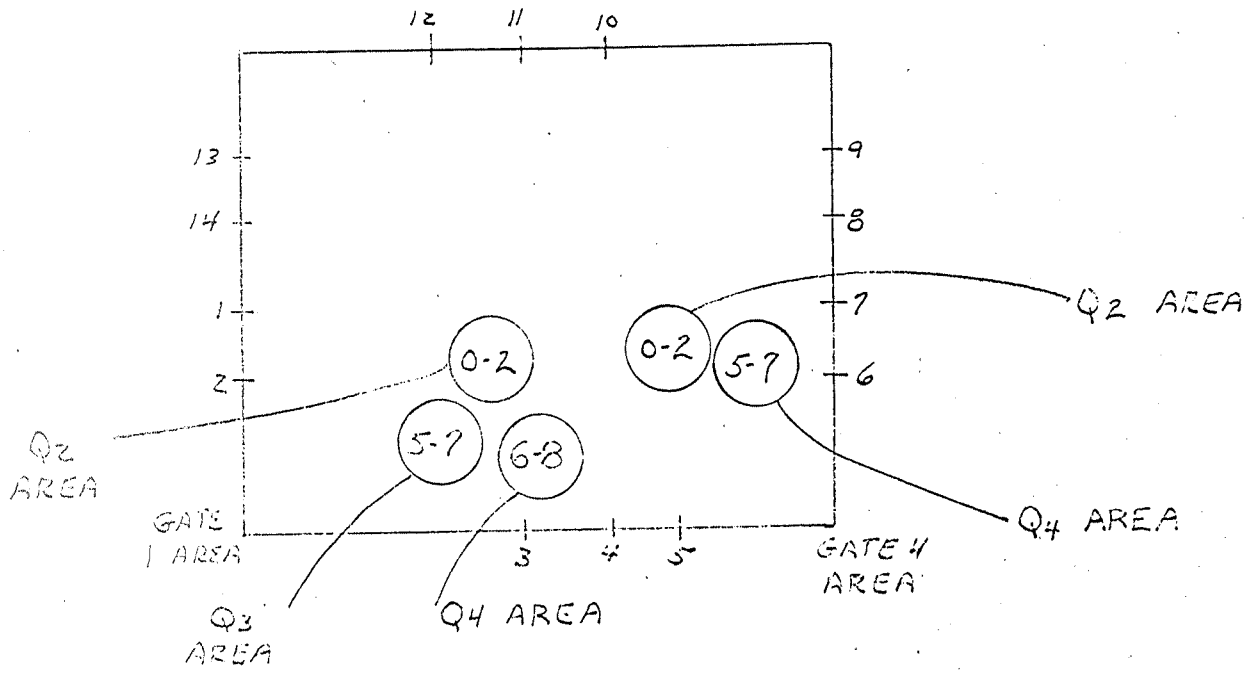


FIGURE 30. TTL Recombination Radiation Map
(Gates 1 & 2 Energized)

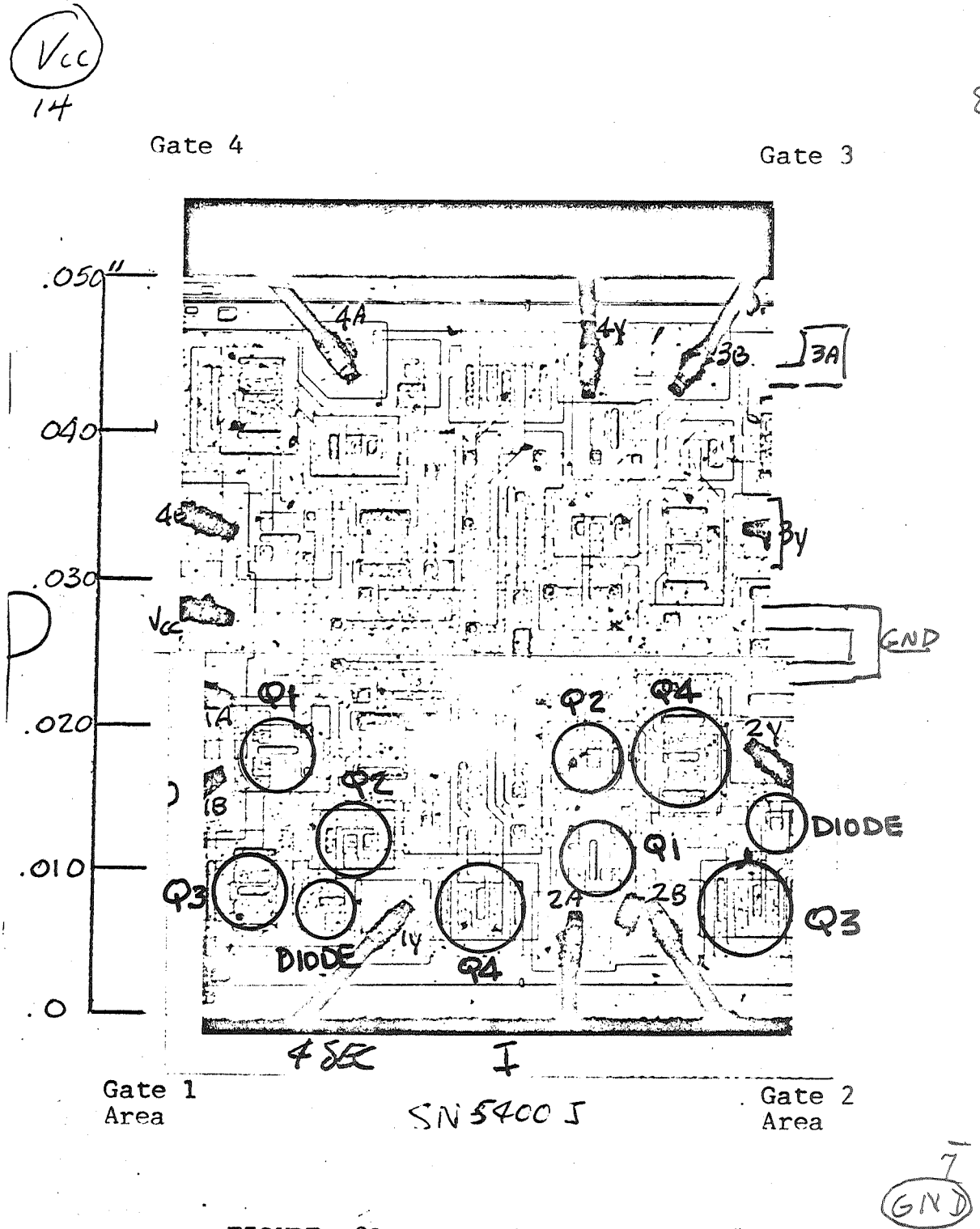


FIGURE 31. Junctions of Gates #1 and 2 Investigated for Recombination Radiation

9.2.1.1 The recombination radiation map of a second test (Figure 32) shows the SJA output when only gate #3 of the device is energized, as indicated in Figure 33.

The schematic device layout (Figure 34) and the component map (Figure 35) show that again, the locations on the radiation map agree fairly well with the component (junction) locations and the levels observed are roughly the same as the previous test with the same input conditions.

9.2.1.2 A third test was made with the SJA utilizing the same input conditions of 2.5v, 20μ seconds, 1k Hz and RL = 1k, but for this test the gates were connected in logic fashion, (Figure 36) in order to electrically energize the TTL device in a different configuration.

Figure 37 shows the recombination radiation measured when the TTL device operates under the conditions of Figure 36. The numbers circled on Figure 37 are the SJA output in millivolts; and Figure 8, the device's component layout, shows good agreement with the location of the observed radiation. Note that gate 1 area shows high radiation; this is due to the increased output transistor (Q4) current in this circuit configuration.

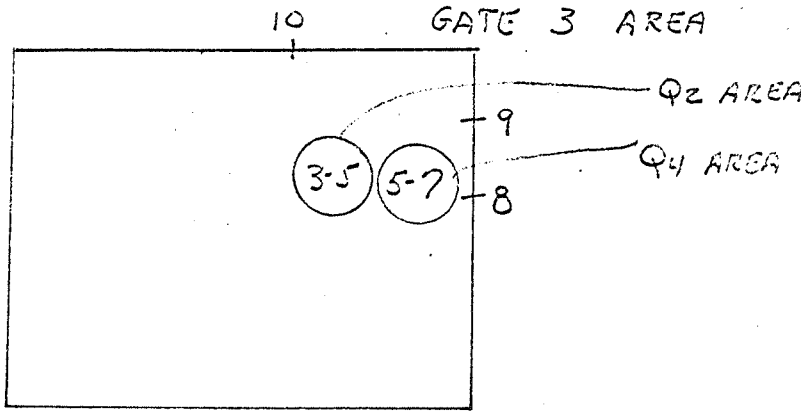


FIGURE 32. TTL Recombination Radiation Map

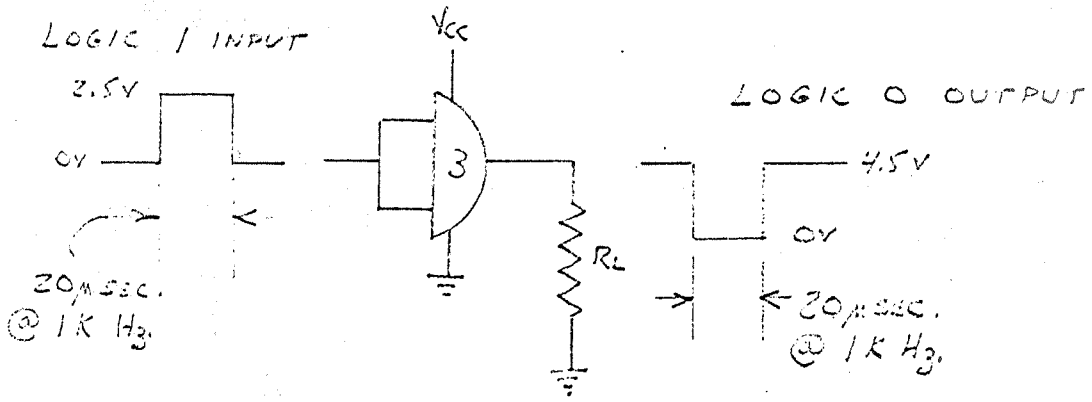


FIGURE 33. TTL Test Setup for Phase 1 Recombination Radiation Study

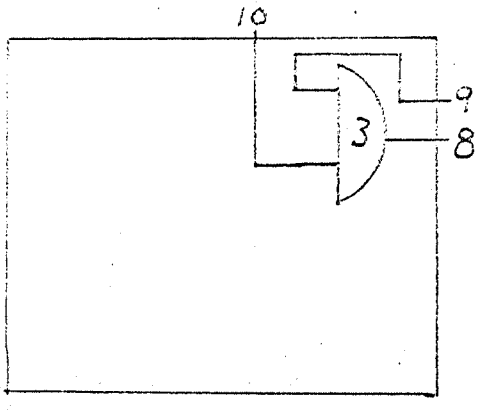


FIGURE 34. Schematic TTL Device Layout, Gate #3 Recombination Test

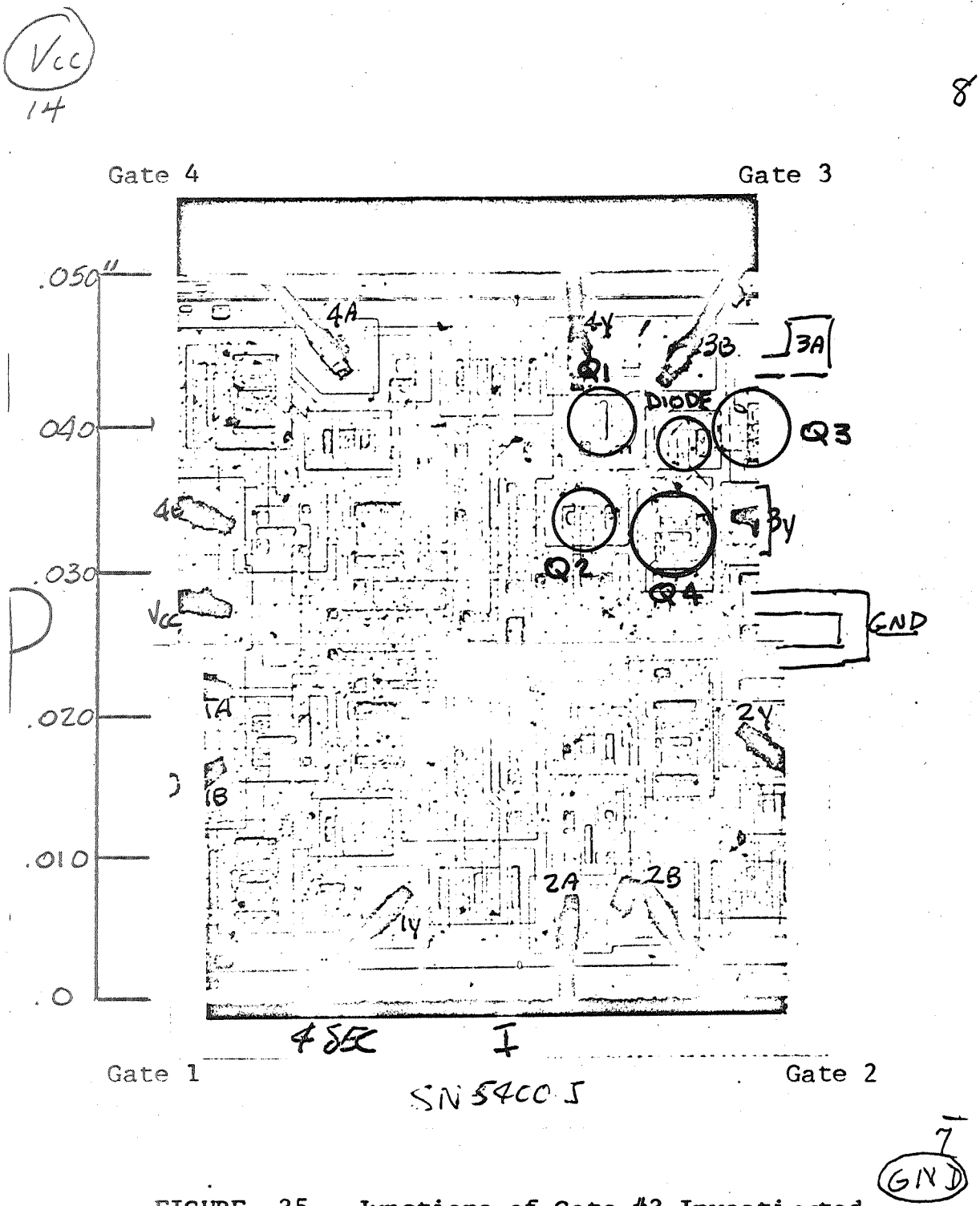
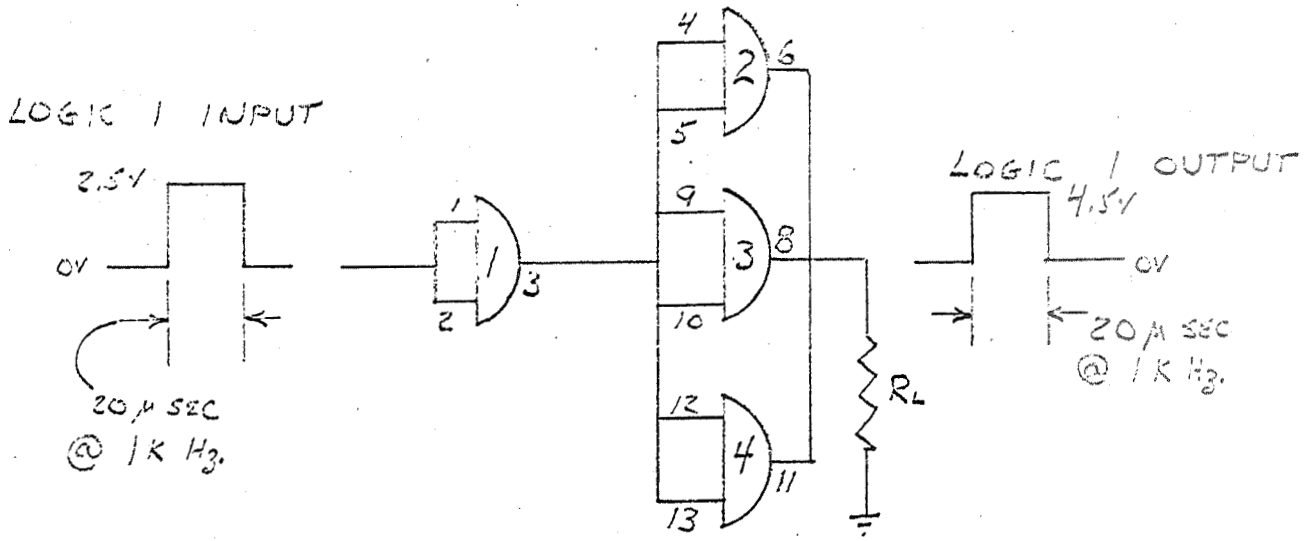


FIGURE 35. Junctions of Gate #3 Investigated for Recombination Radiation



Test Schematic

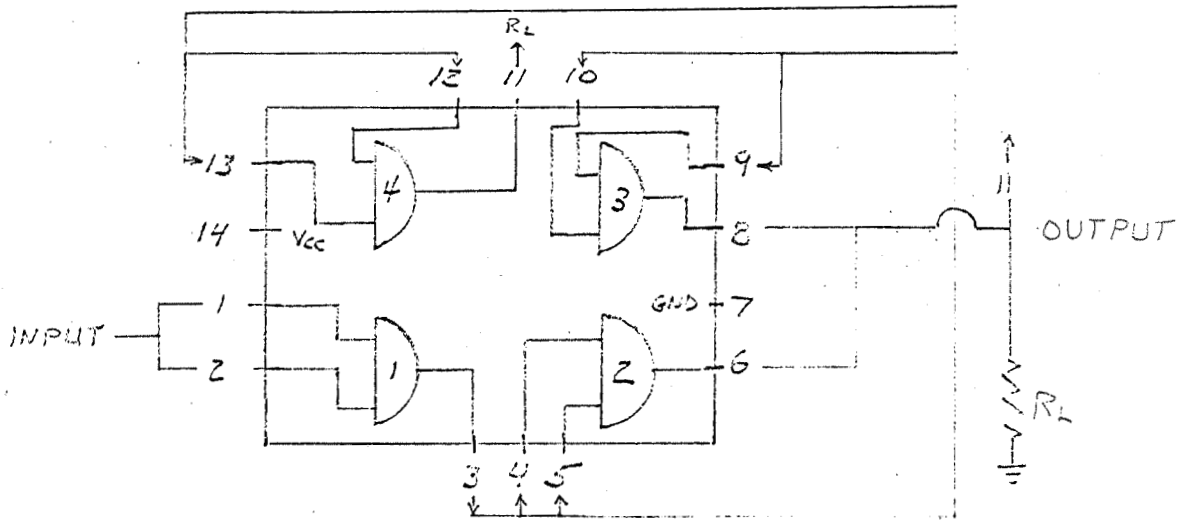


FIGURE 36. TTL Test Setup for Phase 1 Recombination Radiation Study

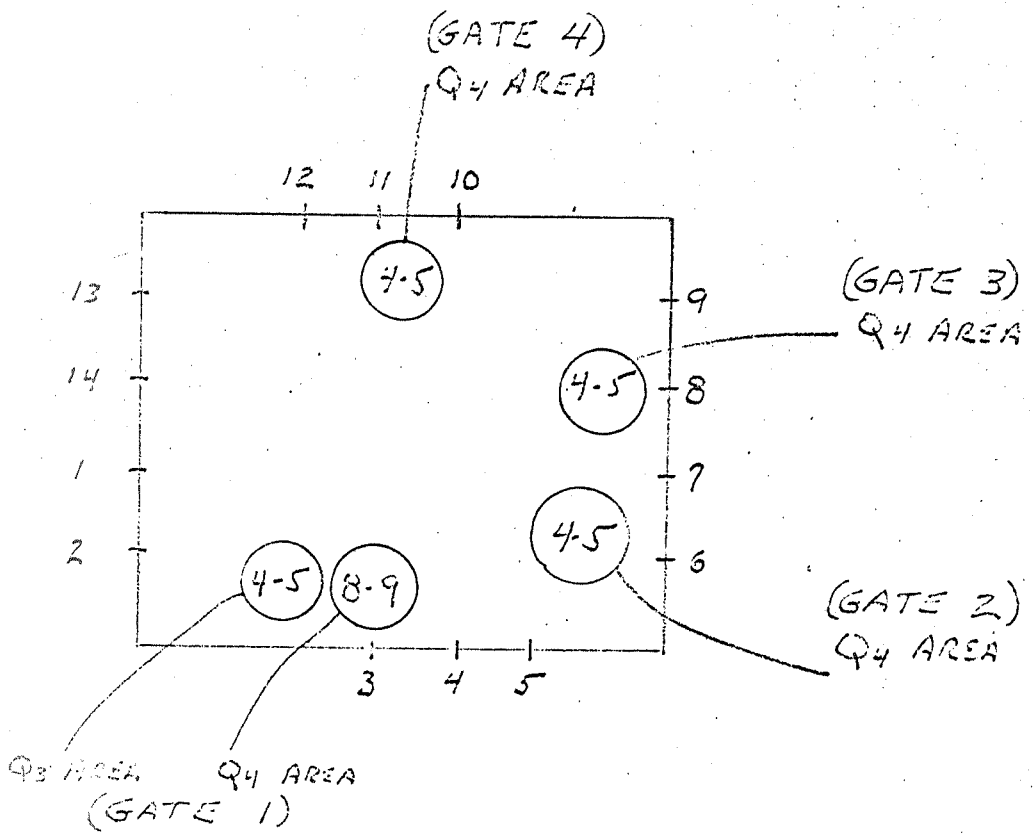


FIGURE 37. TTL Recombination Radiation Map (Logic Configuration)

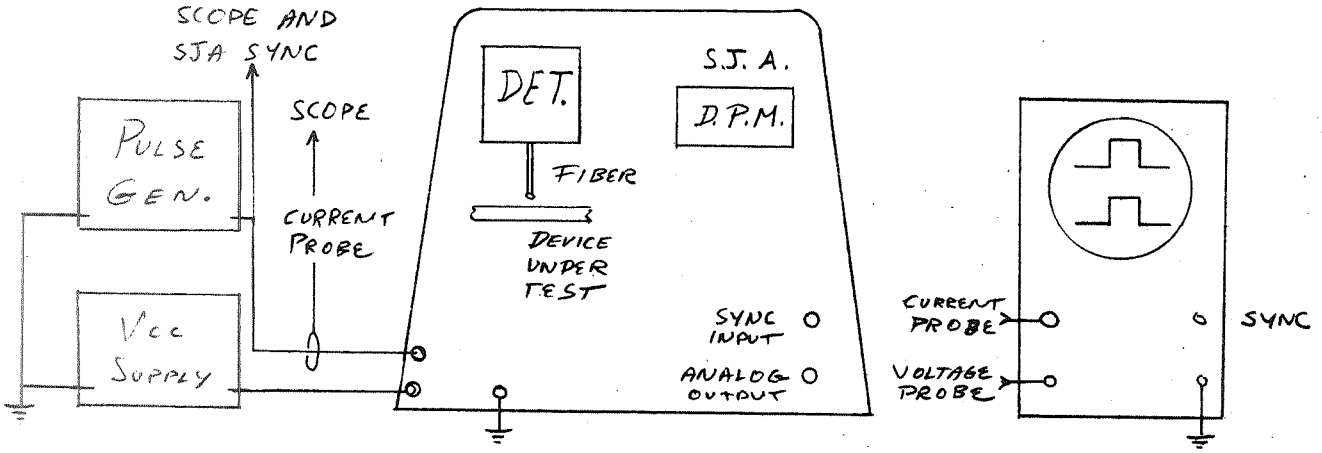


FIGURE 38. Test Setup of TTL Devices for Recombination Radiation Measurement

9.2.1.3 The evidence obtained through the above-described tests led to the conclusion that it is indeed possible to detect and measure recombination radiation emitted by semiconductor junctions of integrated circuits of TTL type.

Phase 1 was therefore considered successfully completed, so that Phase 2 could be initiated on the basis of the preliminary positive evidence gathered in Phase 1.

9.2.2 Phase 2. Measurement Program

The TTL devices, already described in 5.2, were electrically energized as illustrated in Figure 38; namely, the gate under test would be operated as follows: a positive voltage pulse was applied to the input terminal at 1K Hz repetition rate and 20 μsec. pulse width. This pulse serves two purposes. It operates the gate at a low (2%) duty cycle and it gates the Semiconductor Junction Analyzer electronics to "look" at the detected signal only when the test device has switched from Logic 1 to Logic 0. The outputs were not loaded for these tests, and gates 1 to 4 were energized one at a time, as noted in each set of data.

9.2.2.1 TTL Device #3

With gate 1 electrically energized and the .006" fiber aligned with Q2, the readings listed below were obtained:

Input v	Input i (ma)	Digital Meter (mv)
0.0	0.0	0
0.04	0.2	-2
0.10	0.3	-5
0.15	1.0	-10
1.60	1.0	-10
8.00	5.6	-2
8.50	12.0	0
9.00	20.0	11
9.50	30.0	26
<10.00	40.0	43
10.00	50.0	62
>10.00	60.0	90

In order to more accurately locate the radiating junction, a .002" diameter fiber was used for the following readings taken with the fiber located directly above the base-emitter region of Q2:

Input v	Input i (ma)	Digital Meter (mv)
9.0	20	10
<10.0	40	49
>10.0	60	100

The device was now moved so that the .002" fiber was aimed at the base-emitter region of Q4 and the following readings were taken:

Input i (ma)	Digital Meter (mv)
20	6
40	39
60	85

9.2.2.2 TTL Device #3

Gate 2 - the following readings were taken with .006" diameter glass fiber aimed at the base-emitter region of Q2:

Input v	Input Current (ma)	Digital Meter (mv)
0.0	0.0	0-1
0.1	0.3	0-1
0.15	1.0	0-1
1.6	1.0	0-2
8.0	5.5	3
8.5	11.5	4
9.0	20.0	6
9.5	30.0	13
< 10.0	40.0	26
10.0	50.0	40
> 10.0	60.0	55

The fiber was changed for a .002" diameter glass fiber and the following readings were taken looking at the base-emitter region of Q2:

Input Current (ma)	Digital Meter (mv)
20	13
40	19
60	40

while the following readings were taken with the .002" fiber aimed at the base-emitter junction of Q4:

Input Current (ma)	Digital Meter (mv)
20	10
40	16
60	35

9.2.2.3 TTL Device #3

Gate 3 - This gate was inoperative, as evidenced by a quite high input current characteristic.

Also noted was the observance of very negative readings on the Digital Meter, on the order of 30-40mv, present over the entire chip, variable with input current. The gate was also observed as not switching, with the output voltage remaining constant at 4.5V.

9.2.2.4 TTL Device #3

Gate 4 - with a .002" diameter fiber aimed at the base-emitter region of Q2:

Input Current (ma)	Digital Meter (mv)
20	15
40	32
60	67

The following readings were taken with the .002" diameter fiber aimed at the base-emitter region of Q4:

Input i (ma)	Digital Meter (mv)
20	7
40	18
60	40

9.2.2.5 TTL Device #5

Gate 1 - The following readings were taken with a .002" diameter fiber aimed at base-emitter region of Q2:

Input Current (ma)	Digital Meter (mv)
20	15
40	30
60	70

Then with the same .002" fiber aimed at base-emitter region of Q4:

Input Current (ma)	Digital Meter (mv)
20	9
40	20
60	62

9.2.2.6 TTL Device #5

Gate 2 - The following readings were taken with a .002" diameter fiber aimed at base-emitter region of Q2:

Input Current (ma)	Digital Meter (mv)
20	10
40	22
60	53

Then with the same .002" fiber aimed at base-emitter region of Q4:

Input Current (ma)	Digital Meter (mv)
20	9
40	20
60	47

9.2.2.7 TTL Device #5

Gate 3 - This gate was inoperative. The characteristics were very similar to TTL #3, Gate 3, insofar as very high input current and constant output voltage.

9.2.2.8 TTL Device #5

Gate 4 - This gate was inoperative with observations similar to the ones described in 9.2.2.7 above.

9.2.2.9 At the conclusion of this work, all data obtained was evaluated for repeatability and consistency. Following satisfactory verification of the above characteristics, the radiation-current correlation curves of Q2 and Q4 of gate #1, TTL unit #3, were plotted on the chart of Figure 28, as typical of this family of semiconductor devices.

9.3 Recombination Data of LSI Units

These devices have been described in Section 5.3 (See Figure 9). They were to be electrically energized as shown in Figure 29, so as to have them operating in the same mode as the TTL units already measured. In this way, the effect of the additional metallization layers could be evaluated.

This approach is further justified by the comparison of the input characteristics of the two families of devices. These are shown in Figure 39, and they show coincidence up to the "avalanche knee". After this point, the two curves show some divergence, although still retaining a linear behavior. Since these "special units" have been cut off completed and operative LSI circuits, a successful test program would automatically prove the feasibility to measure current flow at any junction of LSI units.

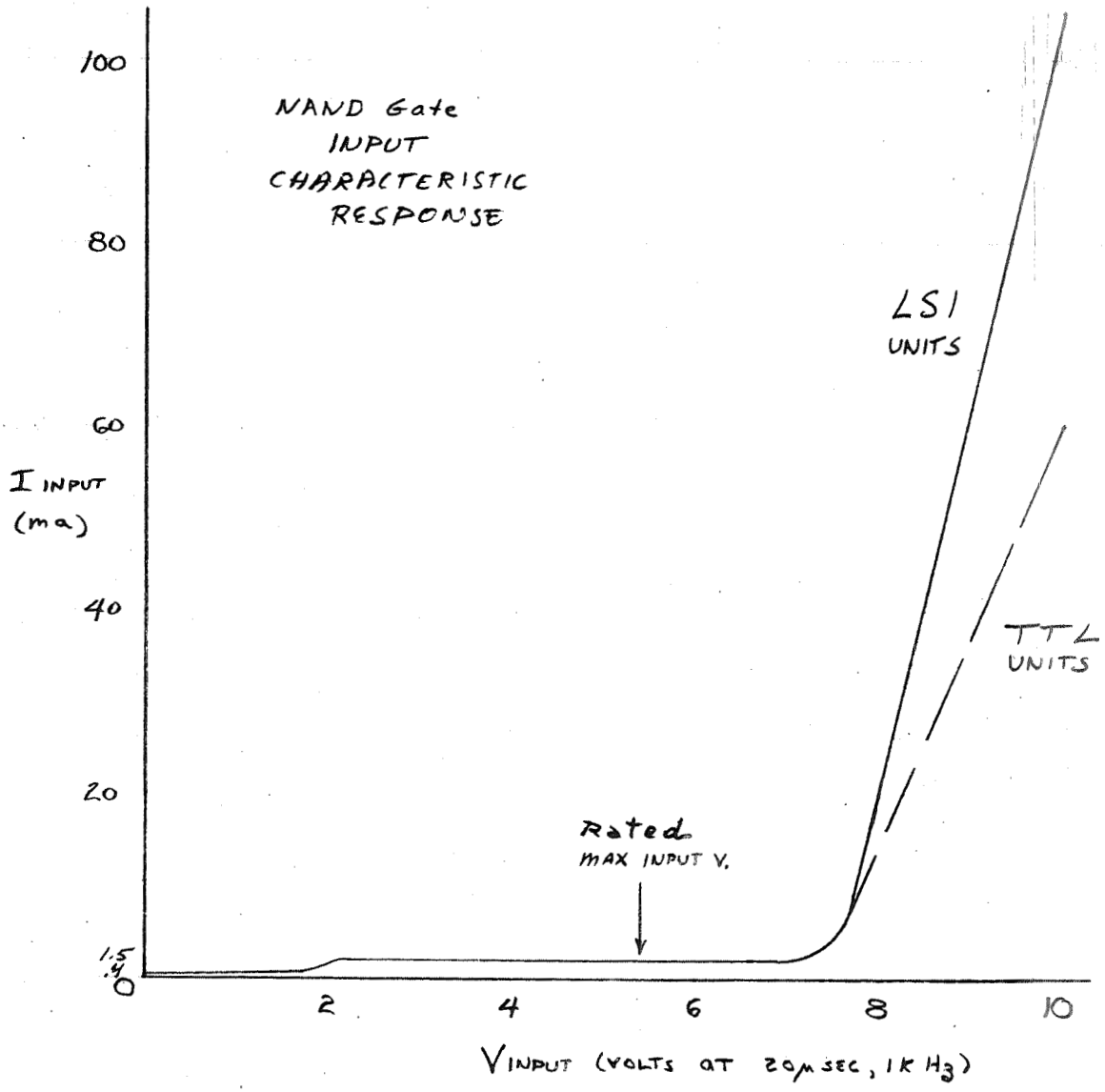


FIGURE 39. NAND Gate - Input Response Characteristics

Four of these "special units" were supplied by Texas Instruments for evaluation. These devices contained various "verified operational" multiple-input gates with schematic as shown in Figure 7, except for the number of inputs. The variation in number of inputs merely makes each of the four devices different in layout and metallization patterns. As far as operational characteristics are concerned, the LSI devices and the TTL units are the same, by design. In particular, units #2 and #6 have two gates each, while units #4 and #5 have one gate each. Figure 9 and Figure 40 to 53 show the visible pictures of these units, taken at various magnification factors, and their electrical schematics.

This unit #2 contains 2 operational cells. #2a is a single input NAND gate.

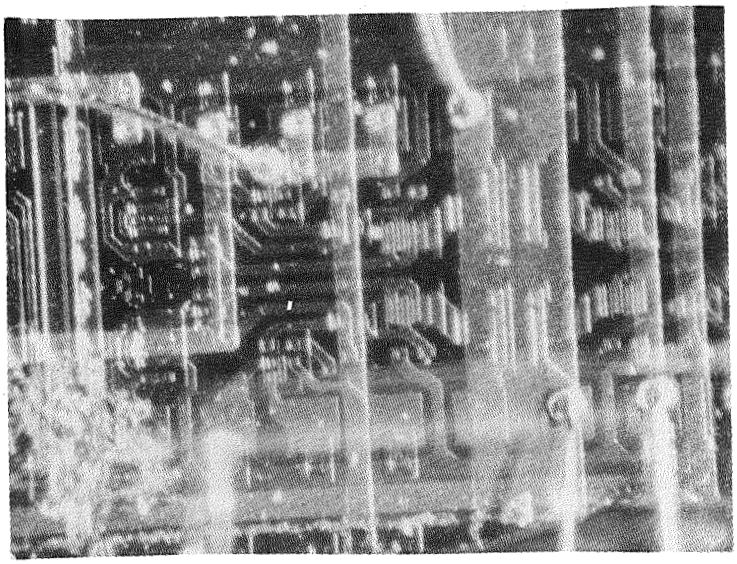


FIGURE 40. LSI Unit #2a (100X)

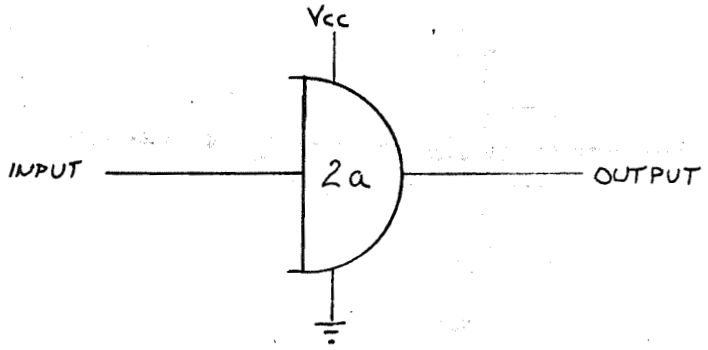


FIGURE 41. LSI Unit #2a (Schematic)

#2b is a 3-input NAND gate connected for use as a single input gate.

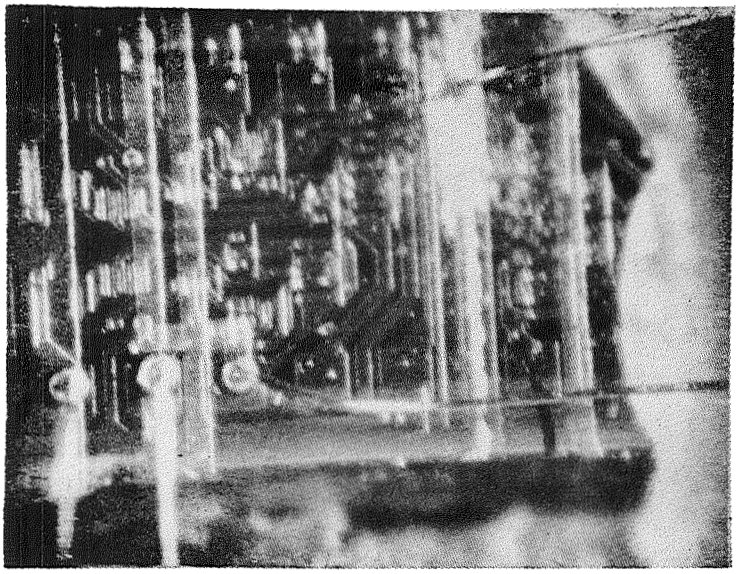


FIGURE 42. LSI Unit 2b (100 X)

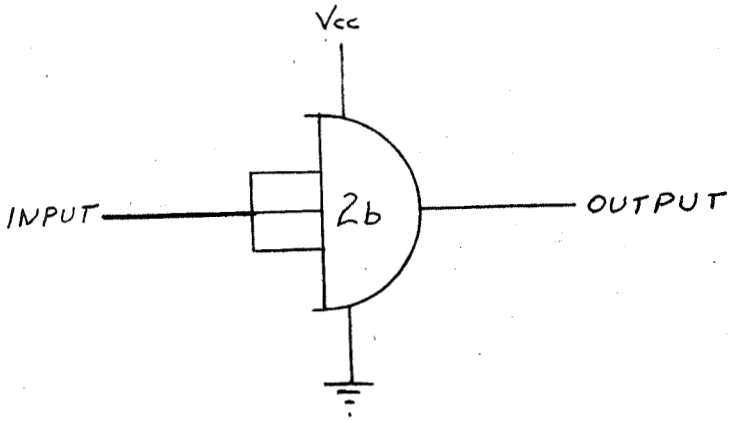


FIGURE 43. LSI Unit #2b (Schematic)

Unit #4 is a 3-input NAND gate connected as a single input gate.

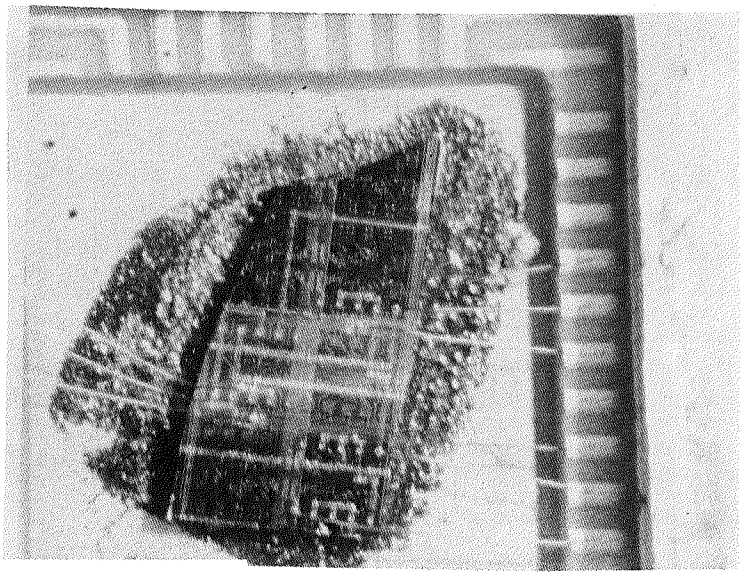


FIGURE 44. LSI Unit #4 (15X)

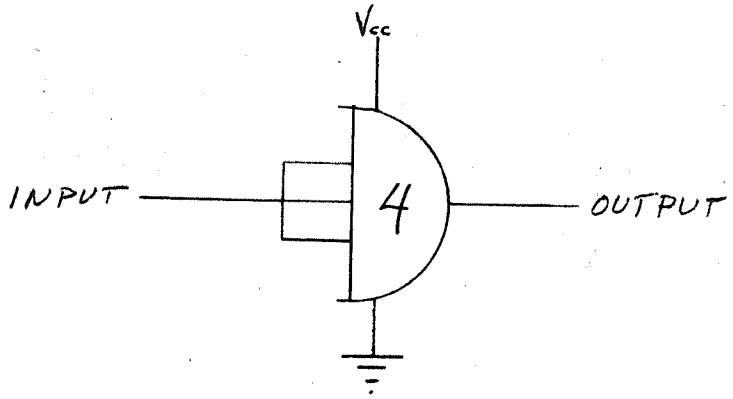


FIGURE 45. LSI Unit #4 (Schematic)

Unit #5 is a 5-input NAND gate connected as a single input gate.

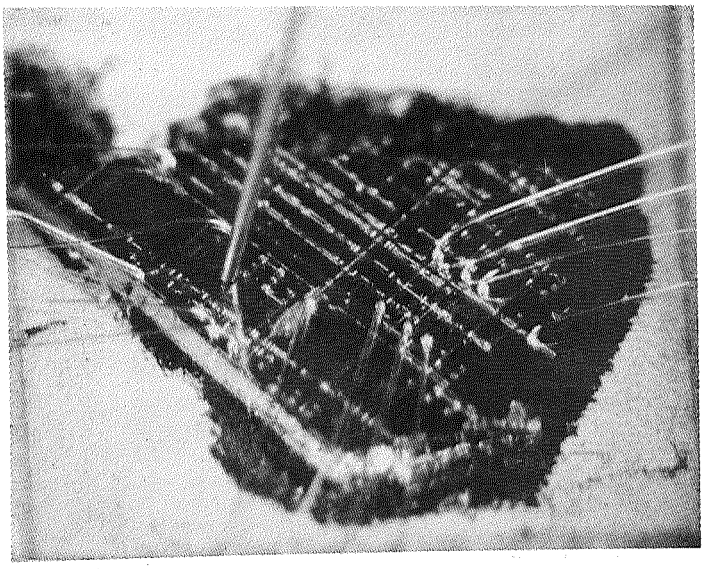


FIGURE 46. LSI Unit #5 (30X)

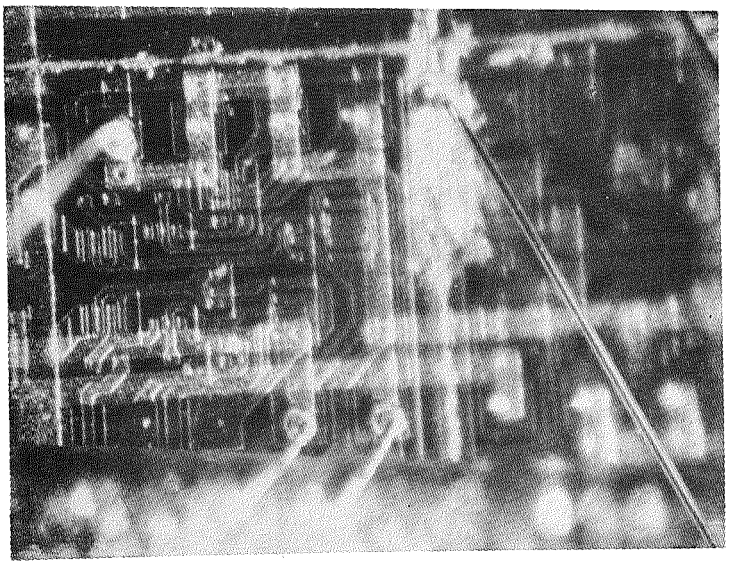


FIGURE 47. LSI Unit #5 (100X)

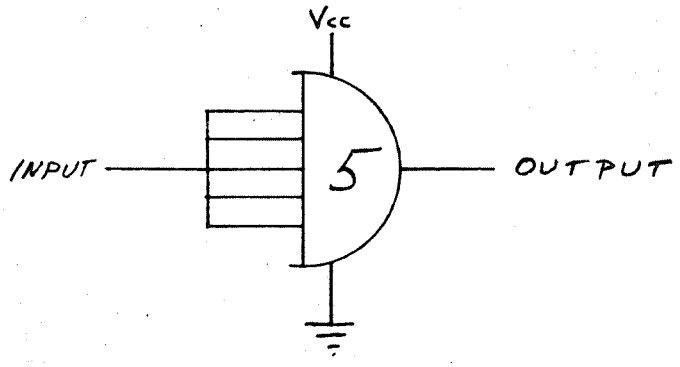


FIGURE 48. LSI Unit #5 (Schematic)

Unit #6 contains two operational cells. #6a is a 2-gate chain of 3-input NAND gates connected as single input gates.

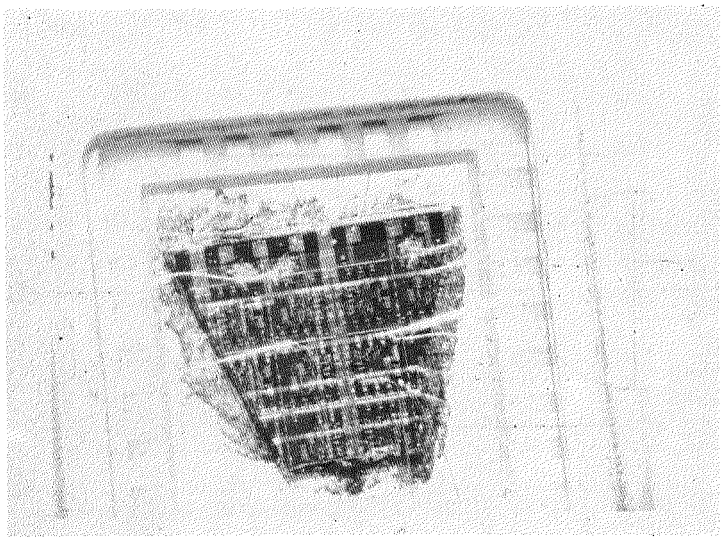


FIGURE 49. LSI Unit #6 (15X)

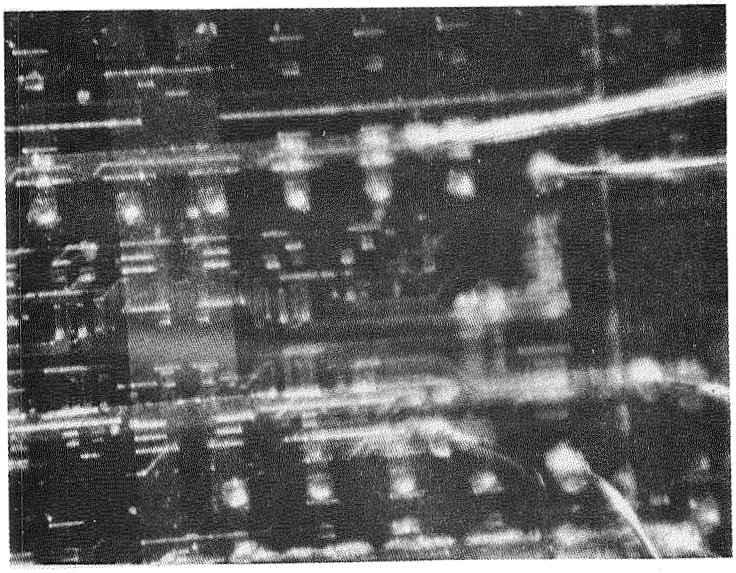


FIGURE 50. LSI Unit #6a (100X)

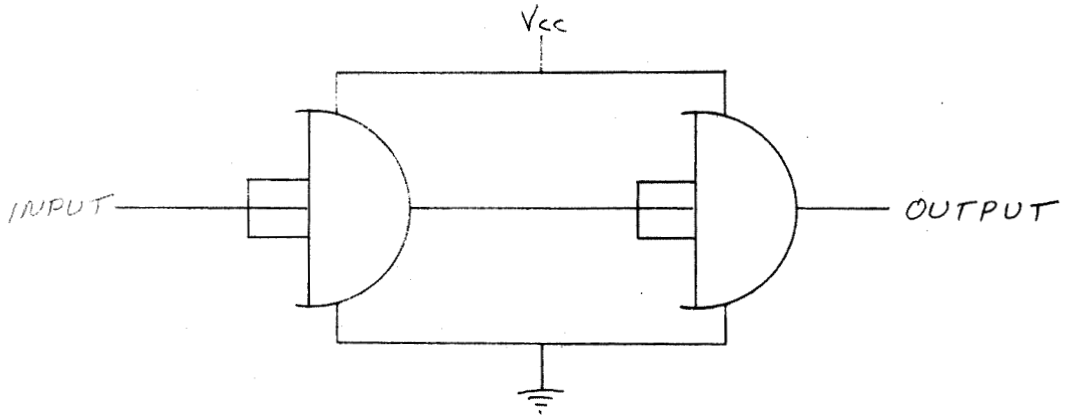


FIGURE 51. LSI Unit #6a (Schematic)

Unit #6b is a single input gate.

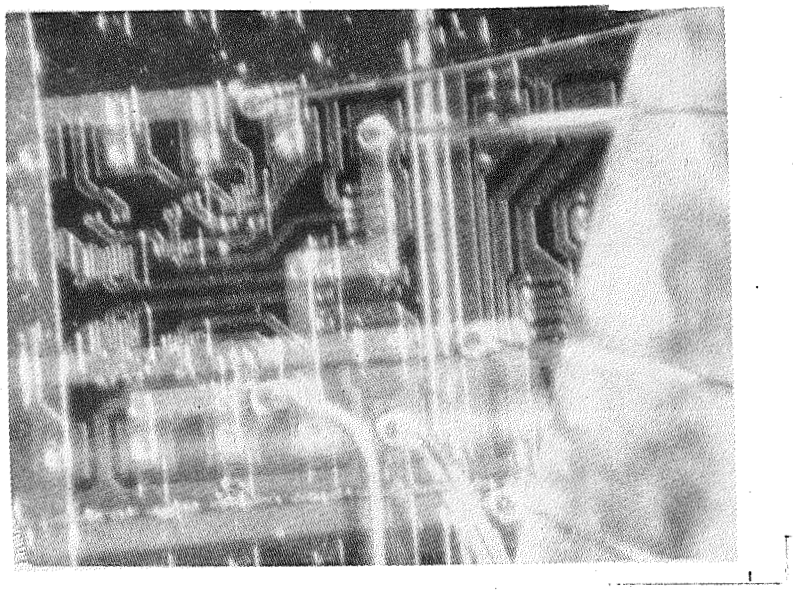


FIGURE 52. LSI Unit #6b (100X)

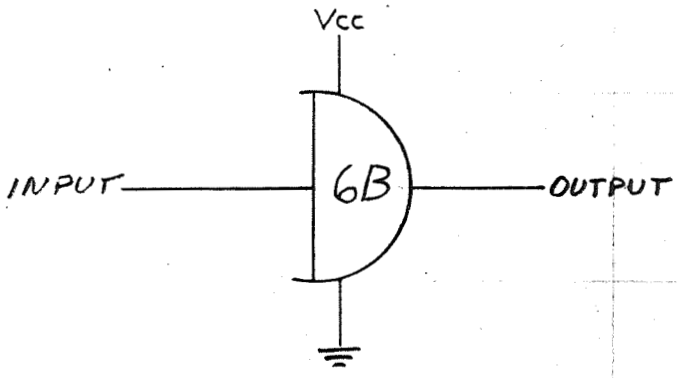


FIGURE 53. LSI Unit #6b (Schematic)

9.3.1 LSI "Special Unit" #2a

The following data was taken with a .006" diameter glass fiber looking at Q4. The input characteristic was verified as conforming to Figure 39:

Input Voltage	Input Current (ma)	Digital Meter (mv)
0	0	0
1.5	1.2	0-2
6.5	1.2	0-2
7.0	6.0	3-4
7.5	10.0	6
8.0	20.0	9
8.5	30.0	13
9.0	40.0	21
9.5	60.0	35
10.0	80.0	57
10.0	100.0	90
10.0	120.0	123

The fiber was replaced with a .002" fiber for the following readings, looking at Q4:

Input Current (ma)	Digital Meter (mv)
1.6	1
8.0	1-2
10.0	3
20.0	6
40.0	10
60.0	18
80.0	26
100.0	39

Then looking at Q2 with the .002" fiber, there was no radiation visible since the base-emitter region is covered with metallization.

9.3.2 LSI "Special Unit"#2b

Initial attempts to locate a radiating junction

were not very successful, although the input characteristic was verified and there was an indication of radiation from the base-emitter region of Q4, but with a .006" diameter fiber, the radiation could not be "peaked" due to the presence of a lead wire. The fiber was replaced with a .002" diameter fiber with the following readings taken, looking at the base-emitter region of Q4:

Input Current (ma)	Digital Meter (mv)
0	0
1.6	0-3
8.0	3
10.0	5
20.0	10
40.0	21
60.0	30
80.0	48
100.0	62
120.0	78

No radiation was observed from Q2 or other components. Q2 was covered with gold metallization.

9.3.3 LSI "Special Unit" #4

This unit was not operating properly. Only 6 ma of input current was obtained at maximum input voltage, and at that level no radiation was evident. The output V remained positive at all times.

9.3.4 LSI "Special Unit" #5

The following readings were taken with a .006" diameter fiber looking at the vicinity of Q3. The

input characteristic was verified as conforming to Figure 39:

Input Current (ma)	Digital Meter (mv)
0	0
2	0
7	0
10	1-2
20	12
40	35
60	55
80	85
100	105

In order to better identify the radiating junction, the .006" diameter fiber was replaced with a .002" diameter fiber and the following readings were taken looking at the base-emitter region of Q2, which was found very close to Q3 on this cell:

Input Current (ma)	Digital Meter (mv)
0	0
1.8	0
10.0	2
20.0	6
40.0	20
60.0	38
80.0	50
100.0	70
120.0	95

9.3.5 LSI "Special Unit" #6a

The following readings were taken with a .006" diameter fiber looking at Q1. The input characteristic was verified as conforming to Figure 39:

Input Current (ma)	Digital Meter (mv)
0	0
1.5	0
8.0	0
10.0	2
20.0	8
40.0	15
60.0	23
80.0	25
100.0	28
120.0	32

In order to identify the radiating junction, the .006" diameter fiber was replaced with a .002" diameter fiber and the following readings were taken, looking at Q1:

Input Current (ma)	Digital Meter (mv)
0	0
1.5	0
7.0	1
10.0	4
20.0	9
40.0	11
60.0	14
80.0	16
100.0	17
120.0	18

The following readings were also taken on Unit #6a after identifying the junctions shown:

Input Current (ma)	Digital Meter (mv)	
	Q2 (b-e)	Q4 (b-e)
0	0	0
1.5	0-1	0
7.0	1	1
10.0	3	2
20.0	12	4
40.0	28	7
60.0	40	11
80.0	44	11
100.0	47	11
120.0	50	11

No radiation was visible from 2nd gate of Unit #6a since most of cell is covered with metallization.

9.3.6 LSI "Special Unit" #6b

The following readings were taken with a .006" diameter fiber looking at Q4. The input characteristic was verified as conforming to Figure 39:

Input Current (ma)	Digital Meter (mv)
0	0
2	0-2
7	4
10	7
20	14
40	33
60	58
80	84
100	150

In order to identify the junction, the .006" diameter fiber was changed to a .002" diameter fiber and the following readings were taken when looking at base-emitter region of Q4:

Input Current (ma)	Digital Meter (mv)
0	0
1.8	0
10.0	2
20.0	6
40.0	15
60.0	30
80.0	45
100.0	66
120.0	84

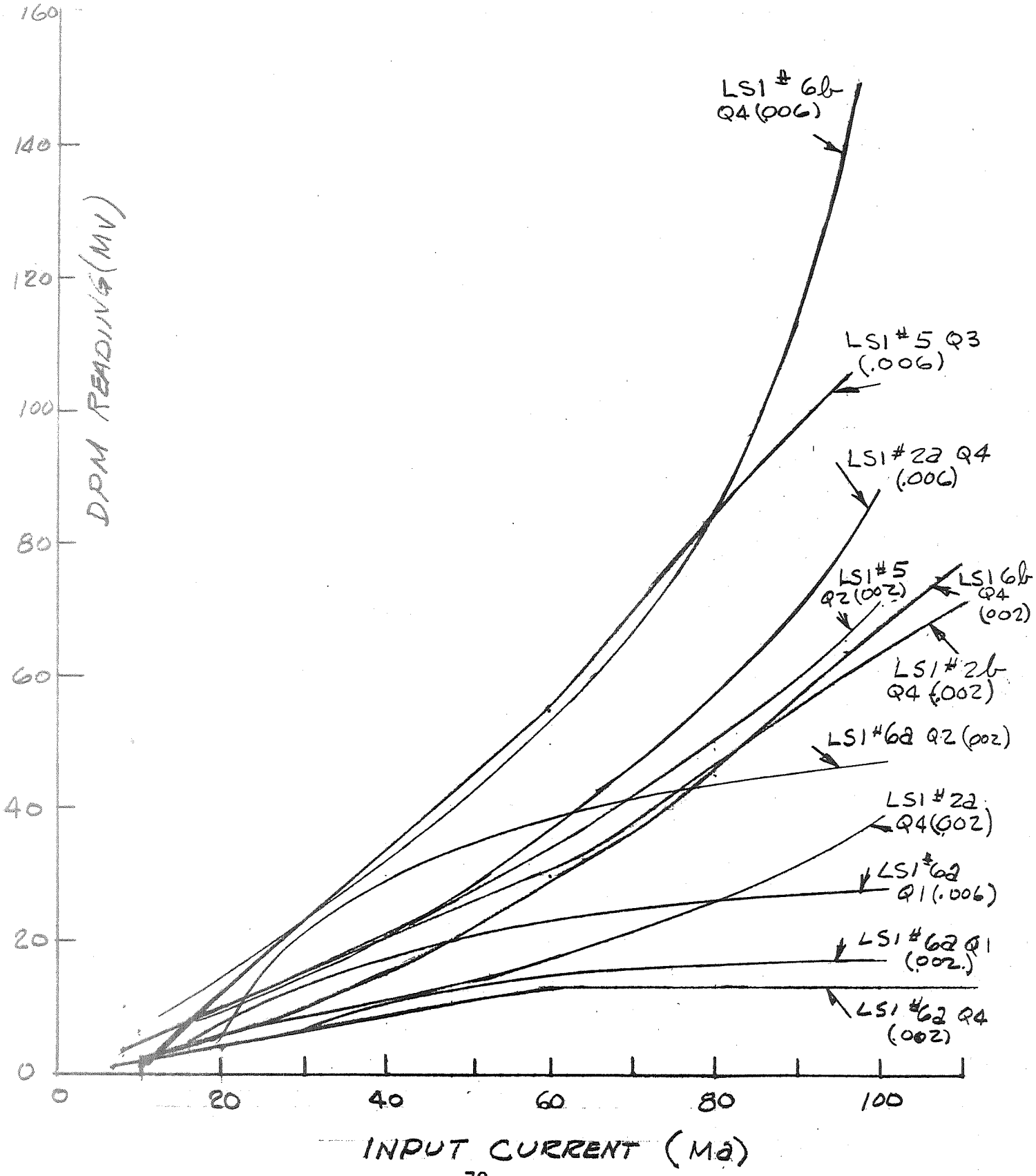
There was no radiation evident at Q2 since the junction was covered by metallization.

9.3.7 At the conclusion of this work, all data obtained was reviewed for repeatability, consistency, and correlation with the data obtained from the TTL devices. The LSI data was plotted in the chart of Figure 54, and it became apparent that the response of unit #6a is different from the response of all other units. This divergence of the radiation characteristic of LSI unit #6a from the general shape of the other unit curves could not be explained. Tests were made putting other gates into the same electrical configuration, but no change of the radiation characteristics of the other units took place. Therefore, it appears as if the odd characteristic of Unit #6a is an intrinsic feature of that unit, and does not depend on the electrical configuration of the circuitry. A rather plausible hypothesis is that it might be caused by anomalies in the forbidden gap of the semiconductor material where the junctions are located.

With the exception of Unit #6a, the response of the LSI units shows satisfactory correlation with the response of the TTL devices. For comparison purposes, the radiation-current correlation curves of LSI units #2a, 5 and 6b have been plotted on the chart of Figure 28, together with those of Unit #6a which shows the anomalous deviation.

FIG. 54

RECOMBINATION RADIATION OF TRANSISTOR JUNCTIONS IN L.S.I. DEVICES Vs INPUT CURRENT



9.3.8 In order to find out what effect the metallization has on the shape of the emitted radiation, the base-emitter junction of Q4 of LSI unit #6b was selected for area and contour measurements.

The data so generated was plotted first in a map configuration, and then a three-dimensional model was derived, as illustrated in Figures 55 and 56. Some asymmetry is apparent, evidently due to the different shape of the metallization in the various areas around the junction.

FIGURE 55

MAP OF RECOMBINATION RADIATION
EMITTED BY Q4 of LSI #6b

DPM READINGS TAKEN AT A DISTANCE
OF .0015" FROM UPPER SURFACE
OF DEVICE

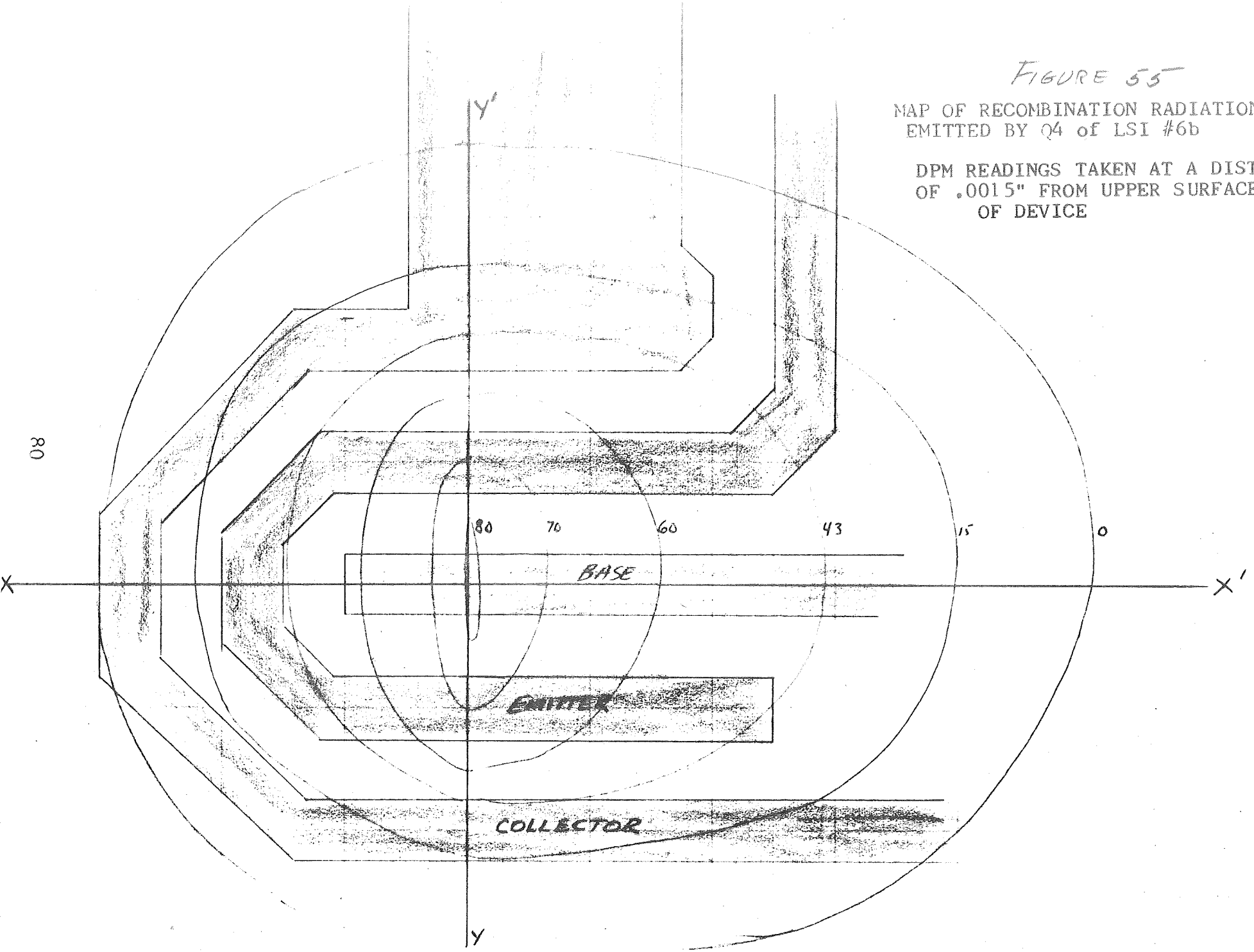


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FIGURE 56

3-D MODEL OF ENVELOPE OF RECOMBINATION RADIATION EMITTED BY Q4 of LSI #6b

10. THERMOCOMPRESSION BONDING STUDY

The goals of this program were to investigate whether infrared techniques could be useful:

A) to assess the quality of the wire bonds connecting the LSI wafer to the outside package terminations, or preferably,

B) to monitor the wire bonding operation so as to assure and control the good quality of the wire bonds while they are being performed.

The major variables affecting the quality of semiconductor wire bonds are the following:

1. collet pressure
2. collet temperature
3. chip temperature
4. chip heat sinking
5. cleanliness of surfaces to be bonded

Of these variables, only those related to temperature could be monitored with the infrared test equipment at our disposal. An effort was made to keep the bonding pressure constant, and to avoid contamination of the surface of the elements to be bonded.

The wire bonding machine used was shown in Figure 16. The gold wire used throughout this work was 0.0007" in diameter,

and several collets for this size wire were supplied by Texas Instrument. Extreme difficulty was met in threading the gold wire through the collet. Further problems were caused by wire clogging in the collet's orifice. All this caused a tremendous amount of time lost in operation setup and performance, to the extent that only a limited number of wire bonds could be considered usable for the program.

Temperature stability measurements, both of the collet and of the substrate (pad), were taken with significant results that are described in Section 10.3.

As a preliminary step, a number of semiconductor chips were needed, on which wire bonds were to be applied. It was thought important to know the quality of the bond between chip and substrate, since it might have an effect on the quality of the subsequent wire bonds. Therefore, it was decided to prepare a number of chips bonded to their substrates with bonds whose quality had been reliably assessed and controlled.

10.1 Chip Bonding & Monitoring

Twenty-four gold-silicon eutectic bonds were made with chips, preforms and substrate supplied by Texas Instrument. The thermocompression bonding machine used was the K & S Model 642, already shown in Figure 15. The bonding operation was monitored with the Vanzetti Thermal

Bond Monitor, Model 1011, already shown in Figure 13. The operational setup is illustrated in Figure 57.

Only one threshold was used, set at 0.3v peak to peak, as read on a Tektronik 535 oscilloscope, and indicated by the green threshold light. All bonds that gave radiation levels above 0.3v were classified as Good, and all bonds that were below 0.3v were classified Poor. For simplicity purposes, only the radiation levels of the poor bonds were recorded in their numerical magnitude, while all bonds exceeding the 0.3v threshold were just recorded as .3+. Three of the poor bonds were very close to 0.3v. These were Nos. 8, 15 and 21. Unit #16 was classified borderline good because it did trigger the threshold level of 0.3v, but took longer than the other good bonds to develop. The following is a tabulation of the bonds and of the Thermal Monitor indications:

#1	Good	.3+	
#2	Good	.3+	
#3	Good	.3+	
#4	Good	.3+	- One corner not bonded
#5	Good	.3+	
#6	Good	.3+	
#7	Bad	.2	
#8	Borderline bad	.28	

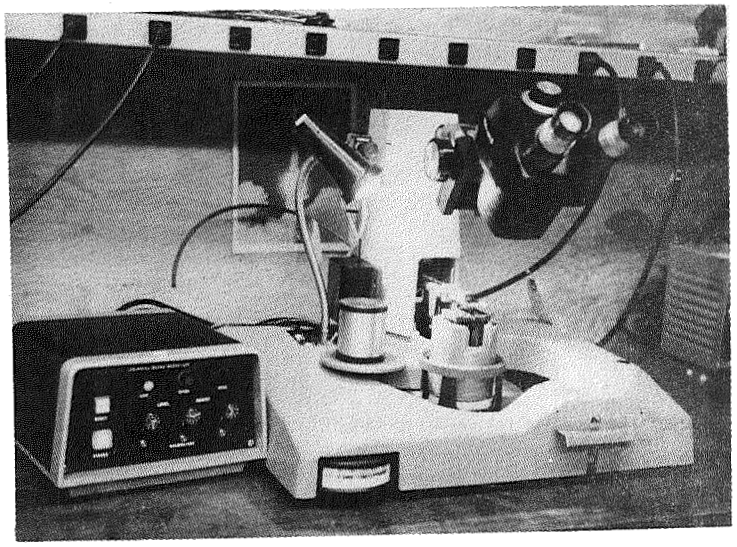

FIGURE 57. Die-Attach Setup with Monitoring Instrumentation

# 9	Good	.3+
#10	Good	.3+
#11	Bad	.1
#12	Bad	.1
#13	Bad	.1
#14	Bad	.2
#15	Borderline Bad	.28
#16	Borderline Good	.3+
#17	Bad	.1
#18	Bad	.2
#19	Good	.3+
#20	Good	.3+
#21	Borderline Bad	.28
#22	Bad	.1
#23	Bad	.1
#24	Bad	.1
#25	Bad	.1
#26	Bad	.1
#27	Bad	.1
#28	Bad	.1
#29	Bad	.1

These units were to be subsequently used for the wire bond tests, as described later in this report.

10.2 Wire Bonding & Monitoring

The original plan was to measure simultaneously the temperature of the collet tip and the temperature of the silicon chip in the area of the pad to which the wire was to be bonded. For this purpose two Thermal Bond Monitors were needed, and Figure 58 shows their setup. Figure 59 and Figure 60 show the position of the two fibers, of which one points to the tip of the bonding collet and the other points to the chip's pad where the bond will be located. While the first one moves up and down with the collet, the second fiber tip is in a fixed position.

Typical instantaneous radiation curves of collet (A) and chip (B) are shown in Figure 61. In order to show them in true relationship, they have been corrected to compensate for the different emissivity coefficients of the surfaces being monitored. Our interpretation of these curves is as follows:

> Prior to the beginning of the operation, the semiconductor chip's temperature is at a steady level, somewhat below the collet's temperature. The collet is also at steady temperature.
>
> As the collet moves towards the chip, its highly reflective surface will reflect more and more of the

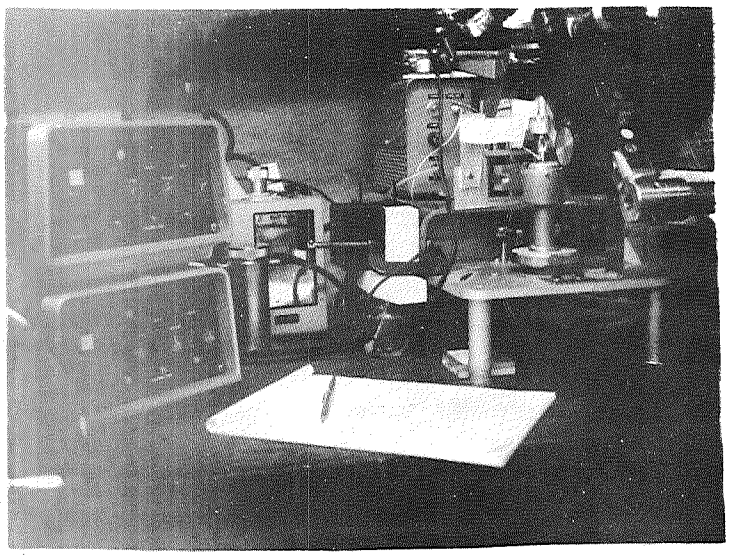

FIGURE 58. Wire Bond Monitoring Setup

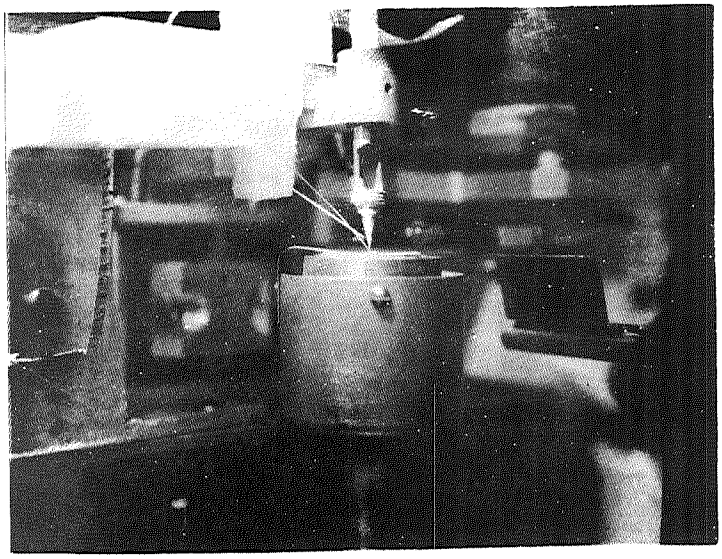

FIGURE 59. Assembly View of Fiber Setup

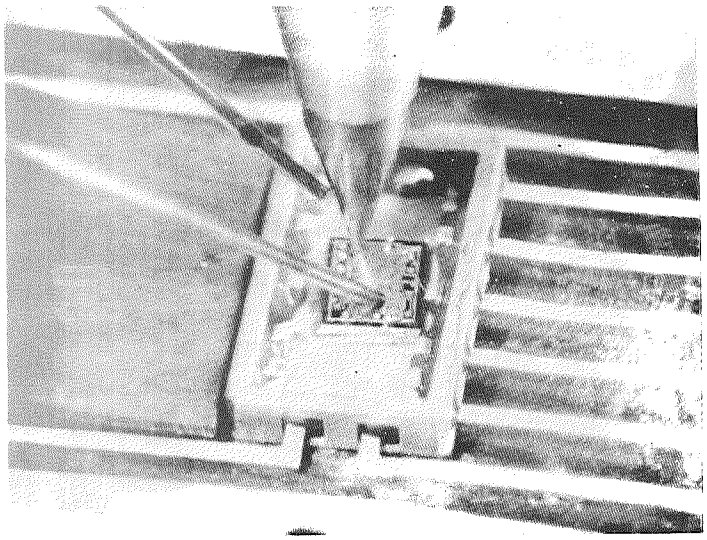

FIGURE 60. Closeup View of Fiber Setup

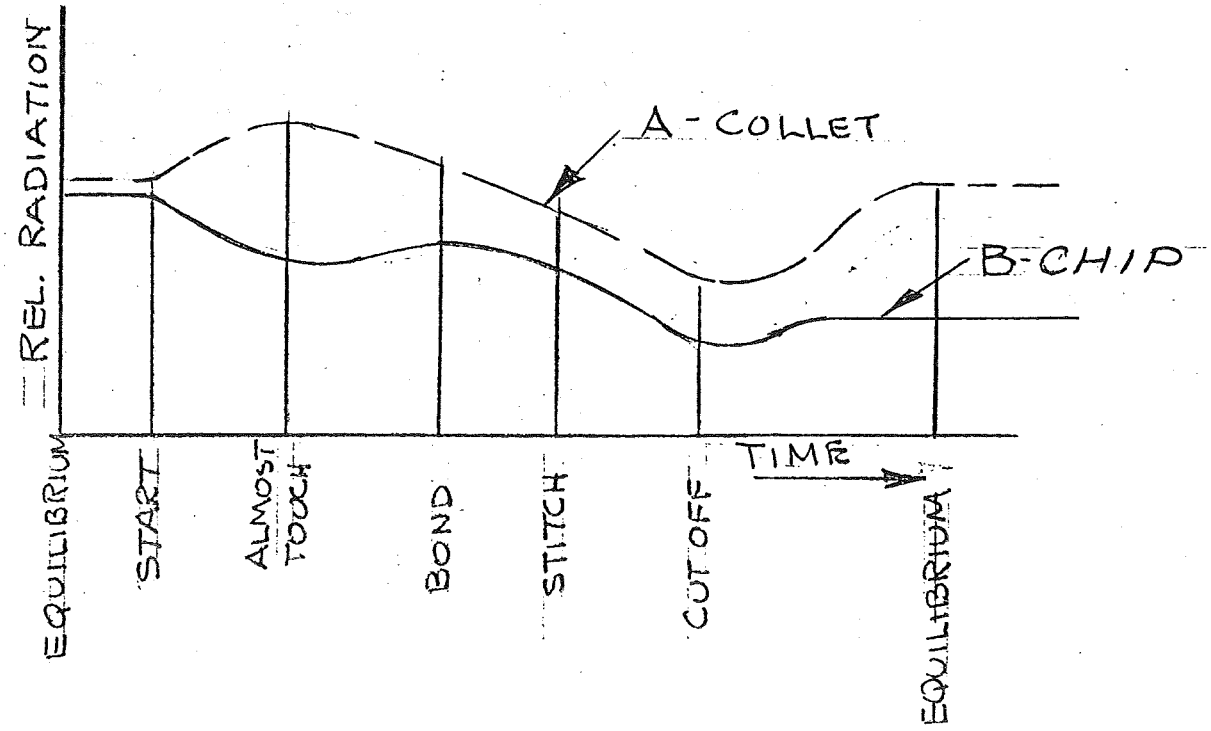

FIGURE 61

VANZETTI INFRARED & COMPUTER SYSTEMS, INC.

COLLET & CHIP RADIATION WAVES

DW'N	SCALE	TOLERANCES: UNLESS OTHERWISE SPECIFIED	DW'G NO.
CH'K'D	MAT'L	FRACTIONAL ± 1/32 DECIMAL .000 ± .005 .00 ± .010	1018A 2001

chip's radiation into the detector's field of view, as shown in the ascending portion of curve A.
At the same time, the field of view of fiber B is being cut by the collet's tip, so that radiation from the chip into fiber B shows a reduction. This results in the descending portion of the beginning of curve B.
At the time of contact between collet and chip, heat transfer between those two elements shows up as a cooling of the collet and a heating of the chip. This is reflected in the related curves.
As the contact is terminated, both the collet and the chip tend to resume their original temperature, but the stitch operation brings both curves at a lower radiation level, probably related to the physical characteristics of the location of the stitch.
Finally, after cutoff, the curves show an initial trend towards their steady radiation levels. These levels should be: for the collet, the same as before the bond; for the chip, a lower level due to the low emissivity factor of the gold bond that now occupies the center of the detector's field of view.

However, repeating this procedure resulted in widespread chip radiation measurements because of fiber movement, which changed the ratio between metallized and non-metallized areas

in the field of view of the detector. The conclusion was that it would be necessary to build a special fiber-holding fixture if we wanted to achieve consistent, repeatable measurements. It was decided that, before engaging in such a complex effort, we should try to monitor the collet tip radiation because, during the cycle, the chip temperature appears reflected in the transient tip temperature, since both elements are in intimate physical contact during the bonding operation.

10.3 At this point the setup was changed to use a Thermal Probe, Model 1017, as shown in Figure 62, for direct reading of collet tip radiation.

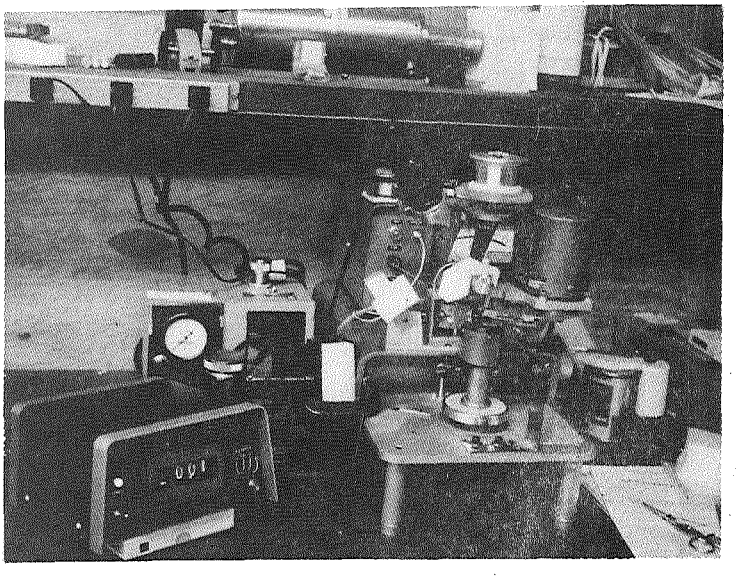

FIGURE 62. Collet Radiation Monitoring with Thermal Probe, Model 1017

The preliminary readings taken on the Thermal Probe were not consistent. Again, it was found that the fiber was moving very slightly, thereby occasionally including some of the background in the field of view. It was then decided to use Sylgard resin between the tip of the collet (side) and the fiber (See sketch in Figure 63) to eliminate background radiation effects. The readings now were consistent and repeatable.

Measurements taken to evaluate the thermal stability of the collet showed wide variations. Figure 64 shows one of the many correlation curves between radiation, temperature, and time during a five minute period. A 30°C maximum excursion in temperature of the tip of the collet is clearly detectable. This could be caused by the cycling of the heat table and by convection currents that can cool the tip drastically. It was noticed that just breathing in proximity of the collet assembly was causing several degrees of cooling in its temperature.

10.3.1 Tests were run to determine the appropriate Variac settings for the collet heater. With the Variac set at 95%, the collet tip temperature was 430°C; with the Variac set at 70%, the collet tip temperature was 260°C. At the 260°C setting, we found we could thread the .0007" gold wire through the collet hole. At the higher setting of 430°C,

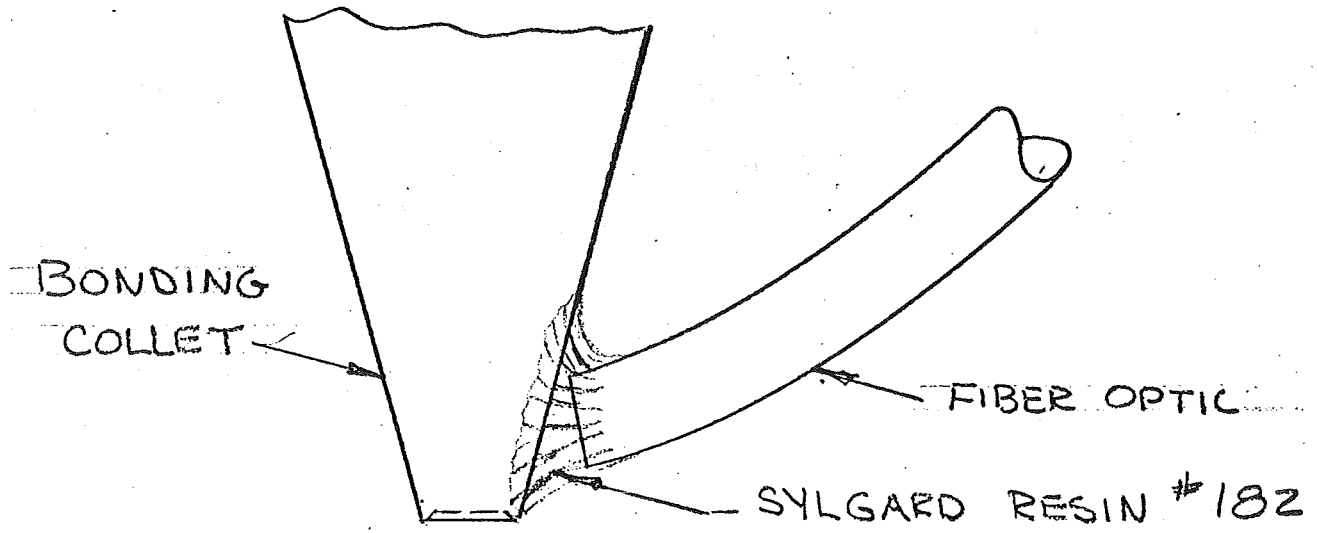

FIGURE 63

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VANZETTI INFRARED & COMPUTER SYSTEMS, INC.			FIBER-COLLET ASSEMBLY
DW'N	SCALE	TOLERANCES: UNLESS OTHERWISE SPECIFIED FRACTIONAL ± 1/32 DECIMAL .000 ± .005 .00 ± .010	DW'G NO. 1019A 2003
CH'K'D	MAT'L		

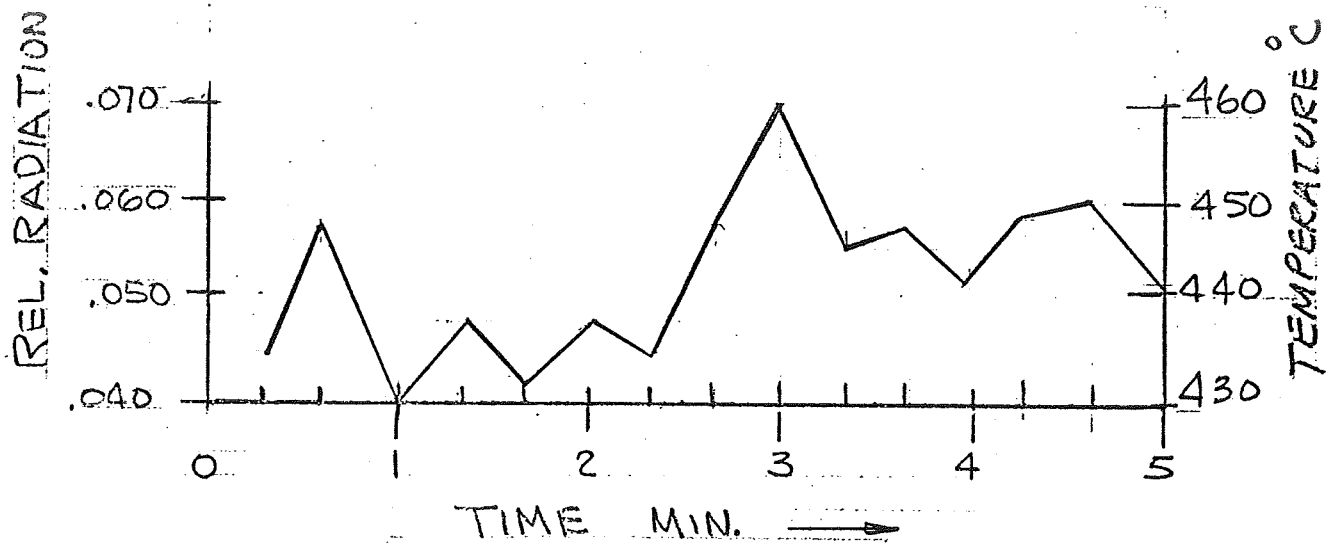


FIG. 6 4

VANZETTI
INFRARED & COMPUTER SYSTEMS, INC.

TEMPERATURE INSTABILITY OF COLLET

DW'N	SCALE	TOLERANCES: UNLESS OTHERWISE SPECIFIED	DW'G NO.
CH'K'D	MAT'L	FRACTIONAL ± 1/32 DECIMAL .000 ± .005 .00 ± .010	1018A 2002

it was impossible for us to thread the wire through the collet hole. Even with the lower setting of 260°C, the wire was consistently pushed back into the collet, due to the bonding pressure on the gold ball; thereby blocking the hole. The wire would then have to be pulled out. A tungsten wire was used to clean the hole every time it became plugged. The gold wire could then be threaded through the hole with a great degree of difficulty. The wire was continuously breaking and blocking the collet, so that we were unable to run a statistically valid number of significant tests.

Measurements were made of the temperature of the collet tip, first with the Thermal Probe and immediately thereafter with a thermocouple applied as per the instructions of the Texas Instrument manual. The results were as follows:

	Thermal Probe	Thermocouple
At a Variac setting of 95%	430°C	290°C
At a Variac setting of 70%	260°C	200°C

These readings mean that the thermocouple acts as a heat sink and cannot be used to reliably measure the tip temperature.

10.3.2 On the chips #25 through #29, wire bonds were attempted. In every case we had difficulty with the wire

breaking and clogging the collet. On unit #26, fourteen bonds were made, and all were acceptable to a pull test that broke the wire before the bond failed. The radiation measured at the tip of the collet with the Thermal Probe for each bond was within 5°C of the optimum temperature. This was accomplished by making a wire bond when the Thermal Probe indicated that the collet had reached the optimum temperature. The corresponding reading on the Thermal Probe was .85 volts, which indicates a collet tip temperature of 260°C, due to the presence of the Sylgard resin, which acts not only as a bonding agent, but also as a emissivity equalizer, so that the detector can read blackbody radiation.

10.3.3 Temperature measurements were made on the hot plate to determine its thermal stability. It was found that in a steady-state condition the hot plate cycled $\pm 5^{\circ}C$ from the set point. The temperature of the hot plate at the center measured 50°C higher with the Thermal Probe, than the thermocouple controller built into the hot plate. Also a gradient of approximately 60°C was found between the center and the edge of the hot plate. This again points to the inadequate precision of the thermocouple readings.

10.4 Results of Bonding Tests

The results of the chip bonding tests were that optimum temperature of bond can be adequately determined with the use of a Thermal Bond Monitor Model 1011. The results of the wire bond tests were that the critical parameter, the collet tip temperature, can be monitored, so that it appears possible to establish radiation standards that are indicative of good quality wire bonds.

11. CONCLUSIONS

As initially planned, work was expended in the following areas:

Thermal evaluation of ICs of the type used in LSI units;
Thermal evaluation of wafer-substrate bond quality;
Correlating current flow through semiconductor junctions with the emitted recombination radiation;
Monitoring the quality of wire bonds during the bonding operation itself.

The results, in synthesis, are as follows:

11.1 Electrically operating ICs and LSIs do have typical infrared profiles. Anomalies that produce variations of the electrical power dissipated by the device are reflected in variations of the infrared profile. However, displaying these variations in a way that could be easily interpreted and routinely processed is the major problem. Lateral heat transfer and emissivity variations add further difficulty to this technique. Any type of infrared scanning microscope can be expected to point out major deviations in power dissipation, both in magnitude and location. However, pinpointing the cause of the deviation, at the component level, will be rather the exception than the rule.

In the particular application to LSI units, infrared fast scanning should be expected to work best at the IC level and not below that size.

11.2 Quality of the bond between wafer and substrate can successfully be assessed with thermal mapping. Minimum size of detectable defect is dependent on the spatial resolution of the scanner. The high thermal conductivity of silicon tends to degrade the resolution. With an instantaneous spot-size of .020", the minimum detectable defect is approximately .080" in diameter.

11.3 The existence of a correlation between current flow through a discrete junction and the recombination radiation emitted by it was verified. For LSI units this means the capability to monitor, without physical contact and in real time, the flow of electrical signals through the different junctions of ICs incorporated in the LSI devices. When these signals are repetitive pulses, they can be read not only in amplitude, but also in waveshape, by using the Waveform Eductor to process the output of the Semiconductor Junction Analyzer.

11.4 Wire bond quality appears dependent on the temperature condition of the tip of the bonding collet. This temperature can be monitored in real time with the Thermal

Probe. A new technique, capable of preventing the formation of poor quality wire bonds, appears now available.

11.5 Statistical verification of all the above-listed results must be obtained, before specifications and procedures are established. However, we feel that the work expended in this program has opened the door for substantial enhancement of the reliability of LSI circuits.

12. RECOMMENDATIONS

The work performed under this contract has verified the existence of good potential for infrared techniques applicable to LSI design and manufacturing for higher reliability in the following areas:

Quality evaluation of the wafer-substrate bond;

Non-contact measurement of current flow through semiconductor junctions;

In process control of wire bonding.

It is our recommendation that further effort be expended in the above-mentioned areas in order to obtain statistical verifications of the findings and to establish performance and resolution limits of the infrared techniques. To obtain this, the following three programs should be planned:

12.1 LSI Wafer-Substrate Bond Quality Evaluation

Using an infrared scanner with at least a resolution of .020", scan a statistically valid number of LSI wafers which have been bonded to their substrates with the inclusion of bond faults of different size, shape, and location. The elements to be established are the following:

a) type of thermal energization to be used

b) thermal gradient to be applied between substrate and wafer

c) area resolution of the faults

d) time constraints of the infrared process, since lateral heat transfer will tend to reduce the area resolution as time goes by.

The infrared scanner best suited for this work is the INSPECT System, not only because of its presently available features, but also because it was designed to accept a laser for instantaneous and localized thermal energization of the target. This approach is explained in Appendix A and it might embody the optimum solution to the problem of infrared bond quality evaluation.

12.2 Current Flow Measurements Through Semiconductor Junctions

Now that the feasibility of measuring the current flow through junctions incorporated in LSI circuits has been demonstrated, a statistically valid program should be carried out to establish the workable limits of the process. In particular, the Semiconductor Junction Analyzer should be used with different size fibers in order to determine for each size junction the area resolution that is necessary. Furthermore, the addition of a Waveform Eductor that can be programmed directly into the Semiconductor Junction Analyzer would provide the investigator with the capability of observing in its true shape the waveform of the

pulses crossing the junction under observation. Elements to be investigated during the recommended program are the following:

a) minimum signal detectable and its correlation to the size of the junction through which it flows

b) optimum fiber size for maximum signal resolution

c) possibility of evaluating uniform working behavior of junctions along the entire length and of detecting points of current crowding and current voids. This should be achieved with the use of fibers whose diameter is smaller than the whole area of the junction so that only partial junction areas can be observed one at a time.

12.3 Wire Bonding Process Control

Verification of the possibility of monitoring the quality of the wire bonds through collet thermal measurement should be carried out on a statistically valid number of wire bonds. The plan should consist of recording on chart the temperature of the collet tip as measured by a Thermal Bond Monitor instrument; after this has been done, pull tests of the wires should be carried out and their strength should be correlated with the data recorded on the chart. In this way upper and lower control limits of

the collet tip could be established, so that they could be applied through a Thermal Bond Monitor instrument for the purpose of process control of wire bonding.

12.4 The above-mentioned three programs, at their successful conclusion, should prove of great value for LSI reliability enhancement, especially in the following areas:

a) Wafer to substrate bond quality evaluation: this is strictly an after-the-fact quality assessment operation. It will be useful to process control engineers and to quality control people. It will enhance the reliability of LSI units, due to the fact that it will enable quality control people to eliminate heating of those parts of LSI units that are located above a bond defect, where the necessary heat sinking is missing.

b) LSI design will be enhanced because the design engineer will be able to follow, both in magnitude and waveform, the signals as they travel through the LSI circuitry. Quality control engineers will be able to make sure that production units meet the performance characteristics of the engineering sample. The capability of spotting points of current crowding and current voids

will also contribute to reduce the failure rate of LSI units.

c) Real time wire bond monitoring will enable manufacturing people to keep the process under control and avoid making defective wire bonds. This again will result in a lower failure ratio and higher reliability.

12.5 An adequate number of LSI units that have been tested with the above-mentioned infrared techniques should then be processed through conventional environmental testing in order to assess in real numbers the reliability enhancement so obtained.

A P P E N D I X A

Proposal for

A FEASIBILITY STUDY

of

A SCANNING HEAT INJECTION SYSTEM

COUPLED WITH A SCANNING INFRARED DETECTION SYSTEM

A FEASIBILITY STUDY

of

A SCANNING HEAT INJECTION SYSTEM COUPLED WITH A SCANNING INFRARED DETECTION SYSTEM

INTRODUCTION

Infrared evaluation of physical targets for material integrity, bonding, and other characteristics requires thermal target energization prior to the infrared measurement. Three methods are currently used to achieve thermal target energization:

1. Heat Flood
2. Heat Soak
3. Heat Transfer

In all three methods the biggest difficulty is posed by the lateral migration of the heat energizing the target. This condition greatly reduces spatial resolution, often masking indications of anomalies that consequently remain undetected.

NOVEL APPROACH

A novel approach for thermal target energization has presently become possible, due to the availability of lasers of various types: it could be called pulsed point heating, such point being either stationary or moving along a pre-established trajectory on the target's surface. This approach eliminates the difficulty due to lateral heat migration, by reducing to a small point the area where heat is injected at every pulse. An infrared radiometer focused on this point will monitor the speed at which the injected heat is being diffused into the surrounding area. Comparing this information with the "expected" characteristic will allow detection of physical anomalies of the material at or near the point of heat injection.

EQUIPMENT

Our company has just completed building a scanning infrared radiometer designed in such a way as to allow the addition of a laser for instantaneous, localized thermal energization of the target. The laser beam is pulsed during the blanking of the detector to avoid unwanted signal pick up by the latter, and is guided by the scanning elements of the optical system, along the same linear path that will be scanned by the infrared detector a fraction of a second later. The system will scan the target either with a single, stationary line, or with a full raster pattern. The operation is schematically illustrated in Figure 1. In A the laser is shown firing a burst of energy during that portion of the spinning mirror's rotation that reflects the heating pulse onto a scan line of the target; during this period of time the infrared detector is blanked out, since its field of view is physically cut by the interposition of the back side of the spinning mirror. After approximately a 90° rotation of the mirror, the detector is shown in B as scanning the same line on the target while the laser is turned off. Variation of the precession interval between heat injection and infrared scanning is made easy by the position adjust control that is partially shown in the illustration.

The major variables of this system are the following, and their optimization should be the goal of the feasibility study proposed herein:

1. wave length and power of laser radiation
2. laser pulse duration
3. speed of scan
4. precession of injection vs. detection
5. size of heating spot
6. emissivity of target surface

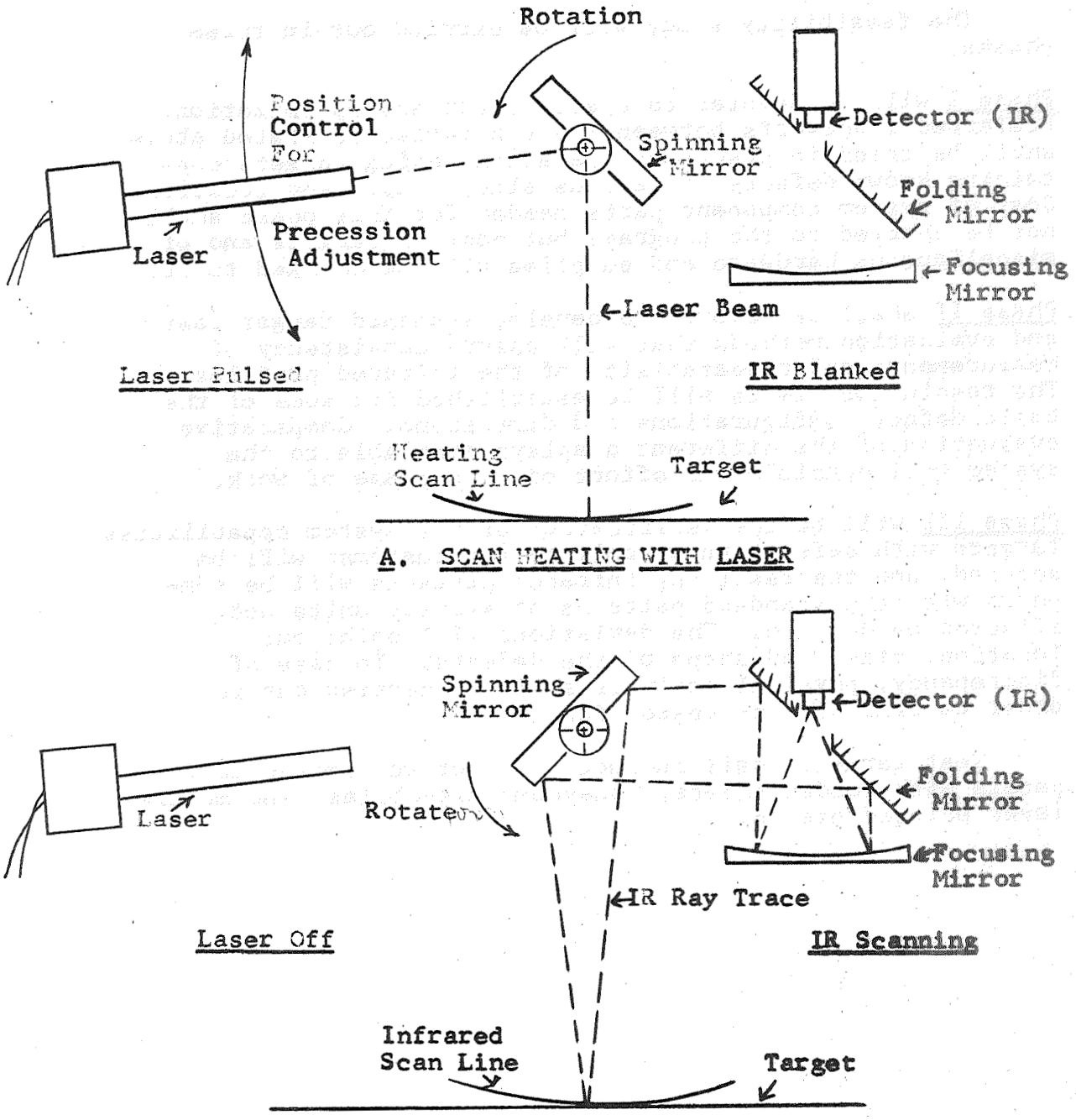


FIGURE 1. SCHEMATIC OF PULSE-INJECTION INFRARED SCANNING SYSTEM

PROPOSED PLAN OF WORK

The feasibility study will be carried out in three phases:

Phase I will be devoted to system setup and optimization. Preferred trade-offs between the six variables listed above shall be tried in practical operation, using targets containing known defects of various size, shape, and location. Cost of system component parts needed for this phase shall not be charged to the program, but cost of targets and of miscellaneous hardware and supplies will be charged to it.

Phase II shall be devoted to develop standard target test and evaluation methods that will assure consistency of measurements and repeatability of the infrared profiles. The resolution limits will be established for some of the basic defect configurations and dimensions. Comparative evaluation of the different displays available to the system will conclude the effort of this phase of work.

Phase III will be the verification of the system capabilities. Targets with defects known only to the customer will be scanned, and the resulting infrared patterns will be compared with the standard patterns of similar units not affected by defects. The deviations will point out location, size, and shape of the defects. In case of discrepancy, physical analysis shall be carried out in order to find out the reason for it.

Test targets shall include, but not be limited to, panels with bonded sheets, honeycomb assemblies, and multilayer printed boards.

REPORTS

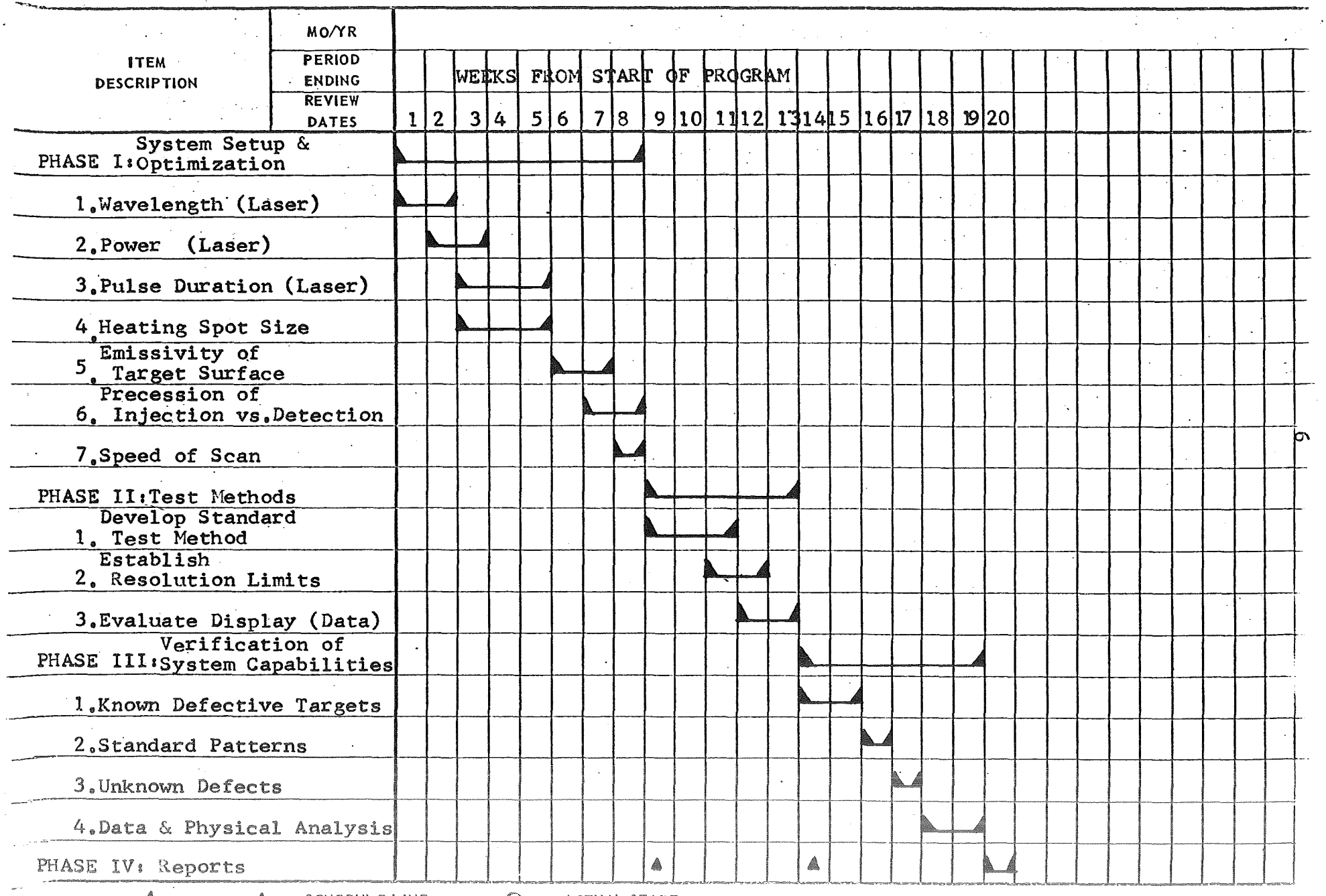
Interim, informal reports shall be written at the end of each phase. They will summarize the work performed, the findings made, and will document the rationale for starting work of the next phase.

A Final Report shall be written at the conclusion of the program. Feasibility of the pulsed point heating approach shall be substantiated with the data obtained in the course of the program. Specifications for infrared test systems having such a capability will be provided. Test methodology will be described in detail and foreseeable applications of the technique listed along with the predictable limitations.

OPTION

After the completion of the program, the customer will have first priority to purchase the infrared system used to carry out the feasibility study at a cost that will not exceed the price at which the same systems will be sold on the commercial market.

RESPONSIBLE ENGR _____ UNIT _____ PROJECT _____ D.O. NO. _____



SYMBOLS: △——△ = SCHEDULE LINE ○ = ACTUAL START
○——△ = PERFORMANCE LINE ○ = ESTIMATED START

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